DAC 2014 | San Francisco, CA | June 5th, 2014

Call for Papers:

DAC Workshop on System-to-Silicon Performance Modeling and Analysis

(http://www2.dac.com/events/eventdetails.aspx?id=170-6-W)

The integration of complex heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional (non-functional) properties and quality attributes of the system like timing, caching, non-determinism, probabilistic effects, power consumption, thermal behavior, reliability, cost and others.

The workshop addresses cross-domain aspects related to the construction of design and verification framework encompassing methodology, interoperable tools, flows, interfaces and standards that will enable for formalization, specification, annotation and refinement of functional and extra-functional properties as well as quality features.

Several research and industry efforts address (parts of) the problem, there is a need of community-wide cooperation to establish common understanding, development directions and proof of applicable solutions. This event will help to create the basis for communication between main actors from system and microelectronics industry, EDA and research.

Topics:

- Requirements and property specification of extra-functional properties (e.g. using UML, SysML, MARTE, …) and multi-physics specification (timing, power, temperature, aging, …)
- Model of computation extensions for non-determinism, probability analysis, caching, timing, power, temperature, reliability, …
- Domain-specific languages / formalisms; system-level design languages (e.g. C++, SystemC, SystemVerilog, …) and extensions to express extra-functional properties
- Platform modelling and abstraction for extra-functional properties from system level, transactional level, to implementation
- System performance exploration and design space exploration using abstract modelling and analysis (e.g. virtual prototyping, …)
    - Power and performance estimation, analysis and measurement techniques
    - Power and temperature aware scheduling & real-time analysis
    - …
- Performance objectives validation
    - Metrics (across abstraction levels)
    - Formal checking of extra-functional properties

Submissions:

Authors are encouraged to outline their work in progress, as short papers (2-4 pages, double column, IEEE format, see http://www.ieee.org/conferences_events/conferences/publishing/templates.html). Submitted papers are required to describe original unpublished work. Submissions must be fully anonymous and authors should not hide previous work, instead, they need to make self-references in third person. Since this workshop addresses true work in progress, authors are encouraged to submit a full paper of their work at another conference.

Papers should be submitted electronically in the PDF format using the EasyChair conference manager:
https://www.easychair.org/conferences/?conf=dacsystemtosilicon14

Publications:

Workshop proceedings of the accepted papers will be distributed to all participants of the event and made available through the ECSI web site. Note that the paper presented at the workshops are NOT disseminated through the official DAC proceedings or through any other formal channels, such as, for example, the IEEExplore or the ACM Digital Library.

Important Dates:

- Paper submission Deadline: April 30th, 2014
- Notification of Acceptance: May 9th, 2014
- Date of Workshop: June 5th, 2014

Organizers:

Kim Grüttner – OFFIS, Germany
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