DAC 2014 | San Francisco, CA | June 5th, 2014

Final Program:

DAC Workshop on System-to-Silicon Performance Modeling and Analysis

(http://www2.dac.com/events/eventdetails.aspx?id=170-6-W)

The integration of complex heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional (non-functional) properties and quality attributes of the system like timing, caching, non-determinism, probabilistic effects, power consumption, thermal behavior, reliability, cost and others.

The workshop addresses cross-domain aspects related to the construction of design and verification framework encompassing methodology, interoperable tools, flows, interfaces and standards that will enable for formalization, specification, annotation and refinement of functional and extra-functional properties as well as quality features.

Several research and industry efforts address (parts of) the problem, there is a need of community-wide cooperation to establish common understanding, development directions and proof of applicable solutions. This event will help to create the basis for communication between main actors from system and microelectronics industry, EDA and research.

Workshop Program	
9:00	**Welcome & Agenda** *Adam Morawiec (ECSI)*
9:15	**Keynote: A System Level Modeling Kit for the Integration of Functional and Extra-functional Properties from High Level Specification Down to Virtual Prototypes** *Laurent Maillet-Contoz (STMicroelectronics, France)*
10:00	**Modelling, Simulation and Analysis of Mixed-Criticality Systems Under Consideration of Extra-functional Properties** *Kim Grüttner (OFFIS, Germany)*
10:45	Coffee Break
11:15	**Model-driven Architecture Exploration, Refinement for HLS and Early SW Development Using Intel® CoFluent™ Studio** *Jerome Lemaitre (Intel, France)*
12:00	**Ageing-aware Virtual Prototyping of MPSoCs** *Olivier Heron and Tanguy Sassolas (CEA LIST&LETI, France)*
12:30	Lunch Break
13:30	**Automotive E/E Architecture Evaluation by High-level Simulation and Hardware Prototyping** *Gregor Walla, Dirk Gabriel, Andreas Barthels, Florian Ruf, Michael Winter, Andreas Herkersdorf (Technical University Munich, Germany) and Hans-Ulrich Michel (BMW, Germany)*
14:00	**VIPPE: Parallel Native Simulation and Performance Analysis for Heterogeneous, Many-core Embedded Systems** *Pablo Sanchez (University of Cantabria, Spain)*
14:30	**Integration of C Source-Level Debugging and HW Tracing and Monitoring** *Shao-Chieh Hou, Hong-Wei Zhuang and Ing-Jer Huang (National Sun Yat-Sen University, Taiwan)*
15:00	Coffee Break
15:30	**Power and Thermal Modeling and Analysis at the System Level** *Gene Matter (DoceaPower, France/USA)*
16:00	**Power Estimation Using Execution Trace Analysis** *Jean-Michel Fernandez (Magillem Design Services, France)*
16:30	**Can There Be a Single Multipurpose ESL Model?** *Yossi Veller (Mentor Graphics, Israel)*
17:00	End

Abstracts of presentations are on the following pages

Organizers:
Kim Grüttner - OFFIS – Institute for Information Technology, Oldenburg, Germany
Laurent Maillet-Contoz - STMicroelectronics, Grenoble, France
Adam Morawiec - ECSI, Grenoble, France

Presentation Abstracts

Keynote: A System Level Modeling Kit for the Integration of Functional and Extra-functional Properties from High Level Specification Down to Virtual Prototypes

Laurent Maillet-Contoz (STMicroelectronics, France)

Abstract: For a decade at least, lots of efforts have been dedicated to the definition of methods and tools to develop pre-silicon platforms (also known as virtual prototypes), to anticipate embedded software development and setup of functional verification framework. Virtual prototyping has proven very useful to reduce time to market, and these platforms are now deployed in the industry. Special interest has risen today in considering extra-functional properties like timing, power and thermal information. This is due to the fact that complex systems integrating more and more complex hardware and software components experience more and more interdependencies between the functional and extra-functional aspects of the system. The ever-increasing complexity of the SoC makes also the overall validation a very complex, time consuming and costly task to achieve. A system wide approach that starts with capturing system level use cases and allows directly deriving test scenarios from these use cases will help to tackle these difficulties. Likewise, it will address the fragmentation of design data which currently causes multiple capture of the same information in different formats, and creates risks of inconsistencies.

In this talk, we introduce a modeling kit and associated toolset as developed in the context of the OpenES project. It provides support of both functional and extra-functional requirements from specification to verification, jointly with the use cases defined at the system level. It also raises reuse capabilities from IP to HW/SW subsystem in order to eliminate integration effort by supporting reuse of pre-integrated and pre-verified subsystems.

Modelling, Simulation and Analysis of Mixed-Criticality Systems Under Consideration of Extra-functional Properties

Kim Grüttner (OFFIS – Institute for Information Technology, Germany)

Abstract: With the predicted device, core and multicore scaling, a recent study revealed that regardless of chip organization and topology, multicore scaling is power limited. It has been predicted that at 22 nm, 21% of a fixed-size chip must be powered off, and at 8 nm, even more than 50%. For mixed-criticality systems, this is of major importance, because safety critical applications cannot be switched on and off or even migrated during runtime. Power and temperature management must guarantee freedom from interference with other applications under all possible conditions. For this reason, the extra-functional properties need to be modelled and analyzed at the system and platform level, because they can strongly affect the overall quality of service (performance, battery lifetime) or even cause the system to fail meeting its real-time and safety requirements. In mixed-criticality systems, cross-application interferences with respect to timing, power and thermal properties need to be captured as well.

In this talk, we present a SystemC-based simulation framework for capturing extra-functional properties in virtual prototyping simulations, currently under development in the CONTREX project. This covers the specification of platform properties (extra-functional model) as well as the dynamic capturing, processing, and extraction of power/temperature information during the simulation. Especially closing the loop back to the application and run-time services is an important feature for complex hardware platforms and software stacks. As an example, we will present a battery-powered mixed-critical avionics system, running a safety-critical flight control application and a performance critical image processing application on the same multicore System on Chip.

Model-driven Architecture Exploration, Refinement for HLS and Early SW Development Using Intel® CoFluent™ Studio

Jerome Lemaitre (Intel, France)

Abstract: Intel Software presents a system-level model-driven approach to structure the design process from HW/SW architecture exploration down to the level of abstraction from which specialized tools can take over. Efficient High Level Synthesis or early SW development in virtual platforms can be achieved. In this flow, architects capture the functional behavior of their system using a SysML* representation or the graphical Intel® CoFluent™ DSL representation. This representation is converted automatically to instrumented transaction-level SystemC* code to provide users with performance predictions in terms of latency, throughput, buffer levels, etc. Then, users map the functional model onto platform models. Platform components are annotated with extra-functional attributes such as power, cost, etc. Users can rapidly simulate and explore performances of multiple mapping alternatives to secure early HW/SW partitioning decisions. Then, users can refine parts of their functional models using Intel® CoFluent™ plug-ins that introduce specific validation rules and generate code for

commercially available HLS tools and virtual platforms.

*Other names and brands may be claimed as the property of others.

Ageing-aware Virtual Prototyping of MPSoCs

Olivier Heron and Tanguy Sassolas (CEA LIST&LETI, France)

Abstract: Chip ageing prediction is becoming necessary to warranty product lifetime while we move to more aggressive process. In this paper we present a work-in-progress to predict BTI effects in MPSoC at early design stages through virtual prototyping. The estimation is based on a lifetime macro-model applied to every component. We implement a C++/SystemC ageing library on the top of an existing MPSoC simulator. This extension collects the internal activity of components and solves ageing equations during the prototyping process. We develop an example of design space exploration that demonstrates the powerful benefit of such capabilities.

Automotive E/E Architecture Evaluation by High-level Simulation and Hardware Prototyping

Gregor Walla, Dirk Gabriel, Andreas Barthels, Florian Ruf, Michael Winter, Andreas Herkersdorf (Technical University Munich) and Hans-Ulrich Michel (BMW) Gregor Walla, Dirk Gabriel, Andreas Barthels, Florian Ruf, Michael Winter, Andreas Herkersdorf (Technical University Munich, Germany) and Hans-Ulrich Michel (BMW, Germany)

Abstract: Most comfort and safety features in a modern vehicle are based on e/e (electric/electronic) systems. This electrification increases with every vehicle generation and contributes nowadays a non neglectable portion to the overall fuel consumption of the vehicle. In this paper we present a framework for the evaluation of e/e architectures with respect to energy-efficiency already in an early phase of the automotive development process. The framework is built around a simulation environment and a real hardware test bench. Experimental results confirmed the validity of our high-level architecture evaluation approach in terms of sufficient accuracy and fidelity in comparison to the implemented hardware reference prototype.

VIPPE: Parallel Native Simulation and Performance Analysis for Heterogeneous, Many-core Embedded Systems

Pablo Sanchez (University of Cantabria, Spain)

Abstract: The FP7 CONTREX project explores the design of mixed-critical systems by developing predictable computing platforms and mechanisms for segregation between applications of different criticalities sharing computing resources. In this context, generation tools create analyzable and executable models of the system from which the functional and extra-functional properties can be estimated and analyzed. Verifying the correctness of multi-processing embedded systems is a complex task. In order to avoid the cost, effort and time that the direct design verification on a physical prototype implies, simulation on a virtual model of the system is the most popular method currently used.

Native simulation technologies have been proposed to generate virtual platforms at the beginning of the design process, reducing porting efforts. As any Discrete-Event simulation technique, native simulation presents problems in order to take advantage of the multi-core architecture of current host workstations where the simulation is going to be executed. Several concurrent simulated threads can be run in parallel in the host but ensuring a deterministic behavior requires synchronizing all them periodically in order to keep causality among events. As a consequence, the number of cores that can be active during simulation is dramatically reduced. Thus, embedded SW performance analysis requires specific simulation techniques in order to efficiently parallelize the simulation and take advantage of the multi-core architecture of the host. In this paper, the results of the research effort towards an efficient, accurate-enough, parallel implementation of native simulation is presented.

Integration of C Source-Level Debugging and HW Tracing and Monitoring

Shao-Chieh Hou, Hong-Wei Zhuang and Ing-Jer Huang (National Sun Yat-Sen University, Taiwan)

Abstract: Debugging both hardware and software for integration is a common thing for a embedded system designer. Debugging a software is friendly for designers. Because of user-friendly interface, break-point/watch-point by C level instructions... etc. However, debugging a hardware is more difficult and complex than debugging a software. Information for hardware debugging is always cycle-by-cycle waveform. User have to find problem in considerable information. It's a big work and always time consuming. Therefore, this paper propose a method to integrate both software and hardware debugging information into the same interface. By adding a wrapper-base in-circuit emulator (WICE) between IP and wrapper and modifying the command in open on-chip debugger (open

OCD) and GDB, we can catch the data from master IP in SoC. Such that cycle-base information can be abstracted into transaction-based information and shows in the same interface - GDB, make user debugging a hardware like software, reduce the time for integration.

Power and Thermal Modeling and Analysis at the System Level

Gene Matter (DoceaPower, France/USA)

Abstract: Energy consumption has become a Key Performance Indicator (KPI) for mobile, automotive, server, networking, embedded and a variety of consumer platforms. Power and thermal behavior directly impact the success of electronic products: cost, reliability, safety, quality of service, user experience, and compliance with industry standards. Power and thermal problems may even threaten brand reputation and limit the acceptance of new design adoption by the industry and consumers. The design technology trend is making power and thermal more and more critical with higher power density, heterogeneous-homogenous multi-core processing and advanced process technology. An ESL approach allows early exploration of power and thermal behavior in advance of real physical systems. An automated approach to building power models coupled with thermal models allows simulation to estimate power as a function of temperature and make better design tradeoffs. When you combine power-thermal models with a dynamic activity from trace behavior or co-simulated with a virtual platform you can develop superior thermal and power management policies for the best user experience. Combining an ESL approach with existing ASIC and system design flows can improve the development, debug and verification to meet or exceed your design targets when you launch your products.

Power Estimation Using Execution Trace Analysis

Jean-Michel Fernandez (Magillem Design Services, France)

Abstract: This presentation will show how it is possible to estimate the power consumption of a system by analyzing the execution trace of a software running on a hardware IP. The presented solution exploits the following assets :

- Software sequence edition: Modelling of the HW/SW interaction through register interfaces and Supporting code generation / execution
- Hardware behavior model: State machine (formal hardware component documentation) and Power profile (state machine annotations)
- Trace replay (Rebuild the history of register accesses)

The models which are used in cooperation are IP-XACT (register databases), MSE (state transitions) and State Machine (support for power annotation).

Can There Be a Single Multipurpose ESL Model?

Yossi Veller (Mentor Graphics, Israel)

Abstract: Electronic system level methodologies focus on the architecture of the design, raising the level of abstraction for design, modeling, and validation to the transaction level. A transaction-level modeling platform provides an essential framework within which many of the essential design and verification tasks can be performed; chief among these being virtual prototyping, hardware verification and validation, and performance analysis. Because the code for the TLM models used to express identical system component behavior varies widely for each of these tasks, the same basic model cannot be used for all of the critical ESL design and verification tasks. This imposes a daunting barrier to the adoption of an ESL flow. Fortunately, this barrier can be surmounted using a methodology built around standard, scalable transaction-level models.