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Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties

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Definition of the industrial evaluation strategy (final)

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History of Changes

ED.	REV.	DATE	PAGES	REASON FOR CHANGES
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SB	2.0	2015-02-27	20	Structure defined
JF, FC	2.1	2015-04-08	24	Intecs contribution
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SB	3.0	2015-04-17	39	Final version
RG	3.1	2015-04-20	39	Final check.

Contents

1 Introduction

This report describes the definition of the industrial evaluation strategy for each of the use cases for the represented domains (this defines at the same time the strategy to evaluate and validate the project outcome with respect to the quantified objectives).

The use-cases can be considered as "CONTREX design flow experiments". Depending on their structure and characteristics, each use-case targets a specific path in the design flow and focuses on a specific tool subset. As an example, the avionics use case focuses on the high-level specifications (based on UML models), while the two other use-cases more specifically focus on implementation and optimization steps. The use cases should provide quantitative metrics to verify the compliance level of the CONTREX methods and tools with regard to the industrial needs and use case goals and objectives. It has been developed in close relation with the use case definition described in D1.2.1 [2] to ensure that all the needs are covered in the evaluation procedures.

1.1 Scope

This deliverable is produced as part of the task T1.3 encompassed by the WP1(defined in the DOW, see [1]), which is aimed:

- To collect the industrials requirements on control in mixed-critical systems for all the represented domains.
- To provide a detailed description of the industrial use cases.
- To define an overall evaluation strategy per use case (domain of D1.3.1).
- To integrate the developed tools and methods into the industrial tools, flows and related standards.

Task T1.3 is particularly focused on the definition of an overall evaluation strategy per use case and how to integrate tools developed in CONTREX scope into.

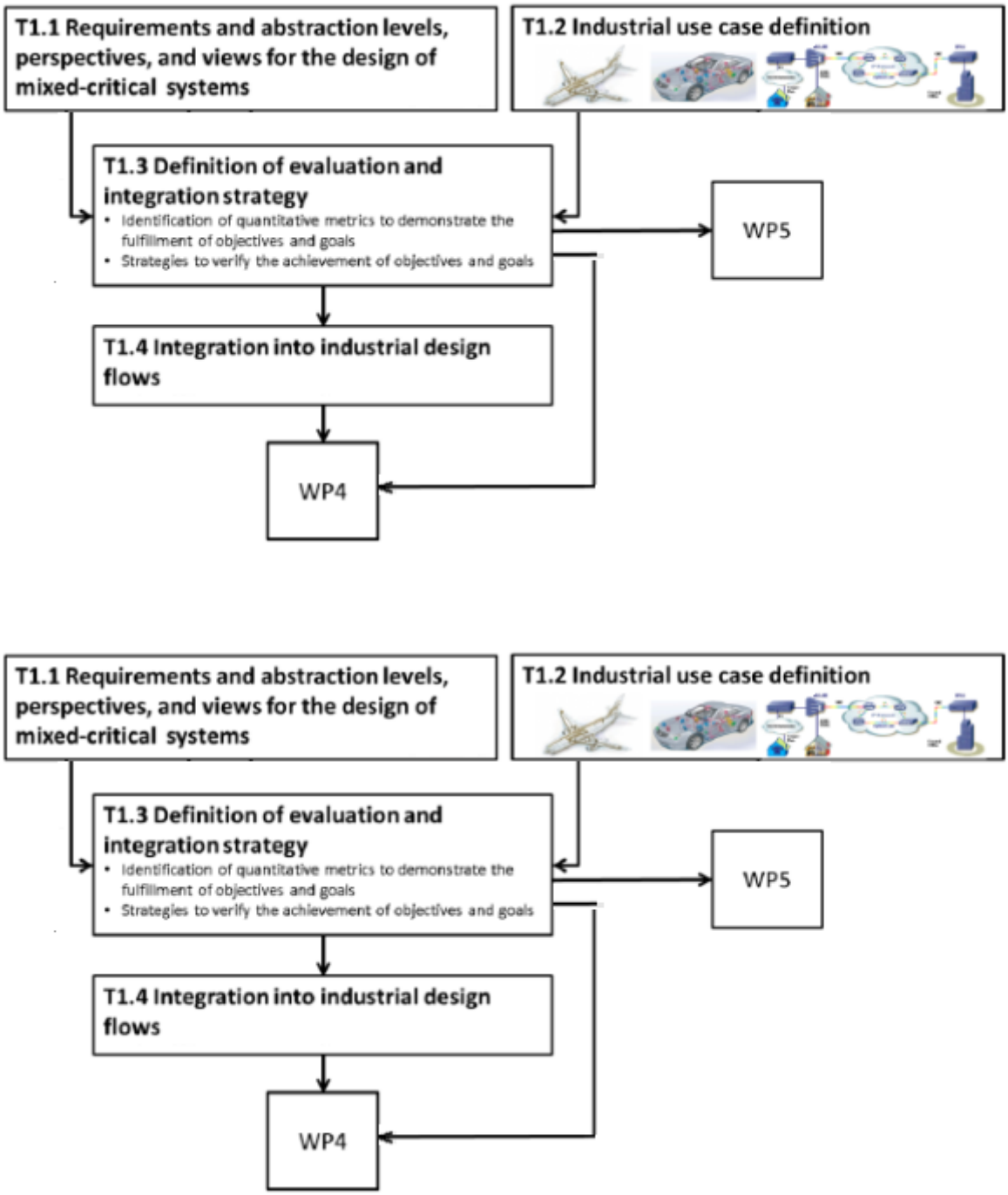

Figure 1. Scope of Task 1.3 into Contrex

1.2 Purpose

Task 1.3 has a specific objective which is to develop a common evaluation methodology to be applied to the three selected use cases. Task 1.3 is led by STM, providing the overall strategy and coordinating the contribution of the industrial partners.

This document presents the methodology that will be followed in order to show the usefulness of CONTREX approach from the perspective of the use case leaders. This plan will include

information on internal milestones, metrics, and templates for the evaluation of the demos, all together forming the CONTREX Evaluation Plan. At the end of the project, together with the finalization of the demonstrators, each use case responsible will provide its evaluation report, to be included it in the correspondent WP5 deliverables.

First objective is to provide quantitative measurements and metrics of the contribution of the technologies developed in CONTREX to the design and implementation of mixed critical embedded systems. The measurement of the benefits of the CONTREX defined technologies in terms of methods, tools, platforms and processes characterisation, definitions and implementations in terms of enhanced efficiency, reduced cost, improved quality and increased competitiveness in the context of mixed criticality, component based, multi-core systems will be addressed.

Second objective is to define the verification strategy to achieve objective and goals of every use case. This evaluation strategy will consist of a set of analysis and/or test procedures against the requirements defined in D1.1.1, describing the necessary inputs, expected outputs and the steps to verify the compliance with the requirements.

1.3 Structure

The structure of this document follows the structure of different evaluation processes defined in CONTREX DoW, therefore the evaluation strategy will be composed of four component:

1. Definition of industrial evaluation strategies of the use cases: once mixed-critical applications will be mapped on execution platforms, validation of the different use cases will take place in task 4.3 based on the requirements defined in D1.2.1. Section 2 describes the validation of the three usecases.

2. Definition of evaluation strategies of models and meta-models and service abstraction from the hardware abstraction layer developed in the use-cases. The evaluation will focus on the integrations of power and temperature models at different abstraction level, that will take place in task 5.1 and it is described in Section 3.

3. Evaluation strategy of the tools developed in WP2 and WP3. Industrial use-cases, which development relies on the use of the proposed tools and methodology, are checked against the key properties identified for each tool family in task 5.2. The common property framework and the key attributes that will be used to evaluate and compare tools to support the hardware and software development are defined in Section 4.

4. The evaluation of the effectiveness of the CONTREX “meet of the middle” approach and the integrability in state-of-the-art flows used in industry are described in Section 5.

Every section is further divided in the different use cases, to collect specific metrics and evaluation strategy.

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2 Evaluation strategies for use cases

Aim of this section is to provide the validation strategies of the three use cases, as described in D.1.2.1 "Definition of industrial use cases" [2]. CONTREX project can be considered as successful only if the flow leads the industrial partners to a satisfying implementations of use-cases. The first step therefore consists in evaluating usecases implementations by using application specific metrics. The objective in this phase of the evaluation is to evaluate the efficiency of the proposed solution and check whether it meets the system requirements edited at the beginning of the developments. The question to be answered in this step is "Does the implemented use cases meets functional and performances requirements?". In that sense the requirements are values that should be monitored and that characterize the implementation in WP4. They can either reflect the intrinsic performances of the design (ratio timing performances / power consumption for example) or its capacity to evaluate the design flow (number of parameters usable by the optimization tool).

Following subsections describe the requirements used for the 3 use-cases

2.1 Avionics domain use case

The following table includes the means of validation of the GMV's avionics use case requirements defined in D1.2.1.

Table 1 Avionics use case requirements

Requirement	**Priority**	**Means of Validation**
AVR-UC01 The demonstrator shall interact with the sensor devices using the appropriate interface. It shall configure each device to generate the required data with the following minimum frequencies: - GNSS receiver: 2 Hz - IMU: 50 Hz - Magnetometer: 10 Hz - Pressure transducers: 10 Hz - Radio Altimeter: 25 Hz ADC Signals: 50 Hz	Mandatory	Functional and performance testing will be carried outfor both simulator and real platform, in order to check whether results are the expected ones and that data are requested and produced at the expected rates achieving all deadlines.
AVR-UC02 The demonstrator shall decode and time-stamp the data received from every sensor device at the minimum frequency specified above.	Mandatory	

AVR-UC03 The demonstrator shall log sensor data at 2Hz.	Mandatory	
AVR-UC04 The power consumption of the demonstrator (including all the components of the selected platform, such as external memory, flash or IO devices) has to be smaller than 5W.	Mandatory	Power consumption measures will be obtained from analysis and simulation tools in order to check whether it is maintained under 5 watt.

2.2 Automotive domain use case

The following table summarizes the means of validation for the Automotive Use Case, as defined in D1.2.1.

Table 2 Automotive use case requirements

Requirement	**Priority**	**Means of Validation**
AUT-UC01 Self-calibration algorithm run-time shall be less than 1ms	Mandatory	Preliminar simulation of the algorithm on cycle accurate ISS, followed by physical measurement during hardware/software integration testing. See (1) and (2) below.
AUT-UC02 Improved crash recognition algorithm run-time shall be less than 1ms	Mandatory	
AUT-UC03 Average power consumption of the sensor node at key-on shall not exceed 80mW	Optional	Preliminar non-functional simulation of the entire node using node-level simulator, followed by physical measurement during hardware/software integration testing. See (3) below.
AUT-UC04 Accelerations sampling frequency during crash recognition shall not be less than 250Hz	Mandatory	Selected acceleration profiles (in the acceleration ranges typical of a real crash) will be generated on a vibrating bench and measures obtained with the sensor node compared againts a high-precision reference sensor. See (4) below.
AUT-UC05 Acceleration range during crash recognition shall not be less than -16g/+16g	Mandatory	
AUT-UC06 Acceleration quantization shall use 12 bit	Mandatory	
AUT-UC07 Acceleration sampling frequency during low-energy event detection shall be less than 100Hz	Optional	Selected acceleration profiles (in the acceleration ranges typical of a low energy event) will be generated on a vibrating bench and measures obtained with the sensor node compared againts a high-precision reference sensor. See (4) below.
AUT-UC08 Acceleration quantization during low-energy event detection shall use 10 bit	Optional	

AUT-UC09 Low energy event detection algorithm run-time shall not exceed 500us	Mandatory	
AUT-UC10 Average power consumption of the sensor node at key-off shall not exceed 30mW	Mandatory	Preliminar non-functional simulation of the entire node using node-level simulator, followed by physical measurement during hardware/software integration testing. See (3) below.
AUT-UC11 Average end-to-end communication overhead shall not exceed 5%.	Optional	Verified at design time. See (5) below.
AUT-UC12 Kura customized code footprint shall not exceed approximately 300Kbytes.	Optional	
AUT-UC13 End-to-end communication latency shall not exceed 30s.	Optional	Experimental verification during in-field valiation. See (6) below.
AUT- UC14 standard protocol shall be adopted for communication between nodes and the cloud infrastructure	Optional	At design time. The system will be designd to fulfill the identified requirements.

In the following, a more detailed description of the approaches that will used for evaluation and that are shortly described in the table above, is given.

1. The KEIL uVision IDE supports cycle-accurate simulation of the firmware on several targets, including the STM microcontroller integrated in the iNemo platform. Thanks to this feature it is possible to obtain a very accurate estimation of the execution time of the analysis algorithms and their dependence on the input data. This is easily feasible since such algorithms do not require real data from the sensors, nor interaction with low-level hardware mechanisms.

2. For all the firmware portion that interact with the hardware devices and for the best possible evaluation of algorithm's performance, physical measurements will be performed by using GPIOs of the device as binary probes, switching at the beginning/end of the relevant activities.

3. The N2Sim simulator will be used to estimate the overall node power consumption in the different operating modes. The simulator is fed with timing estimates (or real measures) of the algorithmic and driver's related portions, power models of the most relevant hardware components and will provide as output both power traces over time and average power consumption figures for each device and for the entire system. Measurement will be performed by averaging the current consumption over sufficiently long time intervals, as instantaneous consumption (i.e. peak power) is not relevant nor critical for the application at hand.

4. Cobra facilities can provide high-performance vibrating benches capable of reproducing acceleration profiles with shot peaks up to 200m/s2. For verifying the

quality of acceleration sampling capabilities of the devices and the correctness of the acquisition, filtering and pre-processing chain, selected acceleration profiles will be reproduced by the vibrating bench onto which one or more Cobra sensor nodes will be mounted, along with a high quality (1KHz sampling rate, +/-24G, 16 bit) sensor, used as golden model. Acceleration measured by the reference sensor will then be processed offline (e.g. with Matlab Signal Processing Toolbox) to reproduce the expected sensor node behavior and compared with the data actually sensed by the iNemo-based node.

5. The overhead is measured as the ration of the size of the information (i.e. the Cobra proprietary protocol packets) generated by the iNemo-based node and the size of the addition data needed for encapsulation. These measures refer to the Application level of the ISO/OSI stack.

6. The overall communication latency will be evaluated artificially reproducing a crash event (a small hit directly on the node is sufficient) and observing the time at which the clod-side application generates the report of the event.

7. Current candidate protocols, both supported by the EUTH Kura platform, are MQTT (see http://mqtt.org) and COAP (see http://coap.technology).

2.3 Telecommunications domain use case

Table 3 Telecommunications use case requirements

Requirement	**Priority**	**Means of validation**
TLC-UC01 Technology provider ofCONTREX shall provide to Intecs lab the Zynq environment (tool chain, kernel,…)	Mandatory	Intecs lab will verify the possibility to generate the Kernel and the Root File System for the Zynq platform, using the environment provided by technology partners
TLC-UC02 The Telecom demonstrator currently running on a MPC880, shall be made runnable on Open Virtual Platform equipped with a reliable model of a Zynq board (the Zynq model must be provided by technological partners)		Several tests will be performed on the Open Virtual Platform in order to verify the correct modelling of the Zynq platform, e.g., verification of the correct implementation of: - Get/set from a MIB browser running on an external PC - web-server connection from external craft terminal - CPU load monitoring This will be a full implementation of the application on the Zynq

		model. The aim is to increase the Intecs Telecom know-how in the usage and exploitation on the Open Virtual Platform, in order to use it in upcoming product development cycles. The objective is to reduce time-to-market by having the possibility to test and dimension the software before final deployment on hardware.
TLC-UC03 Technology provider of CONTREX shall provide to Intecs lab all the peripherals models (e.g. Ethernet interface) to be integrated with the Zynq model on the Open Virtual Platform environment	Mandatory	The Open Virtual Platform setup of the board is executed.
TLC-UC04 Technology partners should provide to Intecs the peripheral model of the memory mapped Hardware registers, with the possibility to develop an applicative software able to read/write that registers.	Optional	Verification of the correct FPGA read/write routines During the original development of the demonstrator Intecs lab experienced many issues with respect to the performance monitoring (data are typically collected every seconds for 15 minutes and then stored in a historical record). A possible test bench would be to verify the ability to manage all the Hardware ticks in 15 minutes without loss of information.
TLC-UC05 The Telecom demonstrator should support the management of 900 Hardware ticks per 15 minutes (an Hardware interrupt per second).	Optional	
TLC-UC06 Technology provider should provide to Intecs an inter-core communication facility for the Zynq dual core platform model on the OVP	Optional	A test bench would be to split the demonstrator tasks between the two cores in order to verify how the CPU load would be affected. E.g. we could move the web server functionalities to the second core and verify that the most critical tasks are no more affected by the web server workload.
TLC-UC07 Power and Thermal analysis tool-set shall be provided and integrated in the Open Virtual Platform by technological partners	Mandatory	Power and thermal computation will be performed exploiting the tool-set provided by the technological partners. The aim is to increase the Intecs Telecom know-how in the usage and

		exploitation on such tool-set, in order to be able to use it in next product developments, having the possibility to estimate the power consumption before to integrate the software development with the hardware one.
TLC-UC08 The Telecom demonstrator, currently running on a MPC880, will be made runnable on a Zynq real board	Optional	The same tests performed on the Virtual Platform, both in terms of functional requirements (registers mapping) that of extra-functional requirements (power consumption) will be performed on a real Zynq platform to verify the: - precision of the modeling of the Zynq on the Open Virtual Platform - the accurate functioning of the power tool-set and its integration in the simulation environment **Note:** This requirement is Optional because there is already a current baseline implementation of the demonstrator running on MPC880 hardware, and thus the porting is principally of interest for cross-verification of the results obtained using the virtual platform and the power/thermal tool-set. Rather than re-engineering the baseline demonstrator *per se*, the primary strategic aim is to use it to provide a basis to extend the company know-how in the CONTREX innovation domains (virtual platform, power estimation) in order to integrate them in future product development processes.

3 Evaluation strategies for models and meta-models and service abstraction

This section collects both common and domain-specific requirements for the specification of mixed-critical systems in the represented domains of the CONTREX project. The question to be answered in this step is "Can the model, meta-model and service abstraction be applied in an industrial context, are the level of detail appropriate, do they lead to real improvement respect to current industrial state of the art?". Use case providers therefore have to evaluate their performances and their degree of adaptation to the industrial needs.

3.1 Avionics domain use case

The following table includes the means of validation of the avionics domain requirements identified in D1.1.1 that are applicable to the modelling language/meta-model.

Table 3.1: Requirements from the avionics domain

Requirement	**Priority**	**Means of Validation**
AVR-M01 CONTREX shall be aligned with the rules and guidelines defined in the D0-178C standard.	Mandatory.	Review of meta-model specification in order to verify that the models that can be generated are in line with the rules and guidelines defined in the standard; i.e., standard's rules and methods are reasonably applicable/verifiable to/against the models.
AVR-M02 CONTREX should use open standards and tools whenever they exist and are suitable.	Optional.	Review of tools used and standards supported and/or followed.
AVR-M03 CONTREXshallsupport a component-based modelling approach.	Mandatory.	Review of meta-model definition in order to verify that it follows a typical component-based approach; i.e., its main entities are components which have certain properties and may interact in several ways. These components must be clearly identifiable in the demonstrator's model.

AVR-M04 CONTREX shall support the modelling of functional, logical and physical characteristics of a system.	Mandatory.	Review of the meta-model definition and its associated semantics in order to check that the necessary entities have been incorporated to the meta-model in order to represent/characterize the functional, logical and physical aspects of the system. The functional, logical and physical aspects of the demonstrator must be representable and clearly identifiable in the corresponding demonstrator's model.
AVR-M05 CONTREX shall support the modelling of usual embedded real-time systems logical entities; such as tasks or shared data.	Mandatory.	This will be verified by reviewing the meta-model definition and checking thatthese entities are actually supported. All the relevant logical entities of the demonstrator must be then representable and clearly identifiable in the demonstrator's model.
AVRM-06 CONTREX shall support the asignment of different levels of criticality to different model components.	Mandatory.	This will be verified by reviewing the meta-model definition and checking that the model components can be assigned, by any means, a specific criticality level, which might be specified for instance using components' properties/attributes or annotation mechanisms. The demonstrator's components criticality levels must be then expressable and clearly identifiable in the demonstrator's model.
AVR-M07 CONTREX shall support the modelling of usual embedded real-time systems physical components; such as processing boards or sensors.	Mandatory.	This will be verified by reviewing the meta-model definition and checking that the se entities are supported. Specific model elements, with precise semantics, for modelling these kind of entities shall exist. The physical components of the demonstrator's platform shall be then representable and clearly identifiable in the model.
AVR-M08 CONTREX shall allow the refinement of the system model across the different development phases, from higher to lower levels of abstraction.	Mandatory.	This will be verified by reviewing the meta-model definition and checkingthat the necessary means to refine the model across the development phases have been included in the definition of the modelling language. These means are expected to consist basically of a set of different abstraction levels that enable the user to model complete systems at different levels of detail, according to the available information at the different development stages.

AVR-M09 CONTREX shall support separation of concerns by means of the definitions of model views and perspectives.	Mandatory.	This will be verified by reviewing the modelling language definition and implementation and checking that a model may be constructed and analyzed from different perspectives and views, i.e., the user of the modelling tools may select at any moment which kind of information from that included in the model should be shown: information concerning time or power consumption, information about the functional, logical or physical aspects of the system, etc.
AVR-M10 CONTREX model views shall be associated to the different extra-functional characteristics of the system under development.	Mandatory.	This will be verified by reviewing the modelling language definition and implementation and checking that the model views match the extra-functional properties considered during the specification of the modelling language (principally time, power and temperature).
AVR-M11 CONTREX model perspectives shall separate the functional, logical and physical characteristics of the system under development.	Mandatory.	This will be verified by reviewing the modelling language definition and implementation and checking that the model perspectives effectively separate the information that concerns the functional, logical and physical aspects of the system.
AVR-M12 CONTREX shall support the assignment of non-functional properties to the model components (e.g. properties regarding time, power andtemperature.)	Mandatory.	This will be verified by reviewing the meta-model definition and checking that the specification of these kind of properties is supported. This specification might done for instance using components' properties/attributes or annotation mechanisms. Demonstrator's extra-functional properties, such as deadlines, periods, WCETsor power consumptions, and constraints on them, shall be expressable in the model.
AVR-M13 CONTREX should support schedulability analysis.	Optional.	This will be verified by reviewing the meta-model definition and checking that all the necessary information to perform schedulability analysis (periods, deadlines, WCETs, etc.) may be added to a given model.

AVR-M14 CONTREX shall allow the allocation of model's logical components onto physical components. These allocations define the design space of the system.	Mandatory.	This will be verified by reviewing the meta-model definition and verifying that model's logical and physical components may be related by some means, in order to specify the (possible) physical realizations of the logical entities and establish a design space suitable for DSE. Thus, the allocation of demonstrator's application components to physical components shall be expressable in the model.
AVR-M15 CONTREX shall allow model-based design space exploration.	Mandatory.	This will be verified by reviewing the meta-model definition and verifying that it provides the necessary constructs to define a design space and enable automatic DSE, without the need of generating a different model for each possible design alternative. For instance, the design space could include the definition of several HW/SW mappings and ranges of values (instead of concrete values) for the explorable parameters, such as processing frequencies. The demonstrator's design space, including all the design alternatives to be explored, must be representable in the model.
AVR-M19 CONTREX shall support the traceability from system requirements to models.	Mandatory.	This will be verified by reviewing the meta-model definition and checking that a method to associate model elements with system requirements has been provided. This method might consist of: - a mechanism that allows to model requirements and then relate them with other model elements created in the successive development phases; - an annotation mechanism that allows to associate comments (including the requiremetn ID or text) to the model entities; or - any other similar mechanism. These associations between model entities and system requirements must be reflected in the demonstrator's model.

3.2 Automotive domain use case

The following table summarizes the requirements and the means of validation related to the modelling activities of the project. Given the complexity of the use-case, several models will be developed and used both at design-time and run-time. In most cases, the evaluation

coincides with availability of tools and software modules implementing the lower-level models.

Table 3.2: Requirements from the automotive domain

Requirement	**Priority**	**Means of Validation**
AUT-M01 general infrastructure for non-functional metric sensing and propagation shall be available	**Mandatory**	Average non-functional figures reported by the customized infrastructure actually executed on the node will be compared against measured data. See description for AUT-01 and AUT-02. See (1) below
AUT-M02 Energy management at node level shall be implemented	Mandatory	At design time. The system will be designed to fulfill the identified requirements. During hardware/software integration testing and in-field validation, changes in the operating mode and (indirectly) on the non-functional aspects involved will be compared to the expected behaviour. See (1) below.
AUT-M03 Mode of operation of the sensing nodes shall be managed autonomously	Manadtory	
AUT-M04 Tradeoffs between energy consumption versus quality of service at node level shall be implemented	Mandatory	
AUT-M05 CONTREX technology providers shall provide coarse grained energy characterization of the iNemo sensor board	Mandatory	At design time: characterization will realized by providing a set of power consumption at different functional modes. During hardware/software integration testing and in-field validation the validation of the energy characterization will be performed. See (2)
AUT-M06 CONTREX technology providers shall provide coarse grained energy characterization of the SeCSoC board	Mandatory	During hardware/software integration testing and in-field validation the validation of the energy characterization will be performed. See (2) below.
AUT-M07 Non-functional simulation of the Cobra sensing node shall be available	**Mandatory**	**The node-level simulator developed by PoliMi will be tested against measured data on the real platform. Due to the technical problems in performing accurate measurements over time with a sufficiently fine temporal resolution, average figures of the different operating modes will be considered. See (1) below.**
AUT-M08 Early estimation of the energy and timing profiles of the sensing node shall be performed	**Mandatory**	

The following list describes and comments the methods used for evaluation of the requirements summarized above.

1. Models, in general, take the form of mathematical equations and their validation on the filed requires implementing suitable software and firmware modules implementing

them. Given that the accuracy of models is already verified as described in Section 2.2, the final validation consists in ascertaining the availability of the software components and their correct integration in the application firmware.

2. Coarse grained models of the iNemo platform and of the SeCSoC platform will be provided by STM and DOCEA (SeCSoC), and STP and POLITO (iNemo). A key point consists in defining and verifying that the class of models developed by technology providers can fit the requirements of the simulation tools and firmware modules used at design- and compile-time.

3.3 Telecommunications domain use case

Table 3.3: Requirements from the telecommunication domain

Requirement	**Priority**	**Means of validation**
TLC-M01 CONTREX shall provide to Intecs a reliable Zynq model to be integrated in the Open Virtual Platform	Mandatory	Verification of the availability of tools, methodologies and related tutorials needed to introduce a modeling layer on the Intecs current design flow This will be verified checking that the model components include the functional properties of the Zynq platform
TLC-M02 CONTREX shall provide to Intecs a reliable model of the main peripherals (e.g. Ethernet interface) to be integrated in the Open Virtual Platform	Mandatory	
TLC-M03CONTREX shall support the assignment of non-functional properties to the model components in the Zynq platform (e.g. properties regarding time and power)	Mandatory	This will be verified by checking that the model components include the mentioned extra-functional properties and that the user may assign them different values.
TLC-M04 Technology provider of CONTREX shall provide to Intecs lab a System Design methodology with the objective to move Telecom system design (i.e. System on Chip, Hardware and Software telecom systems) to	Mandatory	Verification of the consistent mapping between software abstraction and the Intecs current system design. Design constraints and performance parameters must be

a higher level of abstraction		available, such as WCET, maximum memory size, and the like. The strategic objective is to acquire competences in this CONTREX innovation area of modelling and design space exploration in order to allow it to take advantage of modern multi-core technologies in its next generation of products, while keeping critical extra-functional properties (timing, power, thermal) under control.
TLC-M05 The Telecom demonstrator must be representable by a concurrent process network diagram, with no shared state or side effects.	Mandatory	
TLC-M06 Technology providers must provide to Intecs the necessary tutorial and support to acquire all the necessary background knowledge on tools suitable for design space exploration (e.g. Forsyde methodology, SystemC language, etc.)	Mandatory	
TLC-M07CONTREX technology partners should provide to Intecs a tool-set for model-to-model transformation from Forsyde/SystemC to UML/MARTE languages, in order to improve theIntecs system modelling simulation environment	Optional	This will be verified by checking that the model components include all the relevant functional properties of the Telecom application

4 Evaluation strategies of the tools

This section collects both common and domain-specific requirements for the specification of mixed-critical systems in the represented domains of the CONTREX project. The question to be answered in this step is "Can the tools be applied in an industrial context, do they lead to real improvement respect to current industrial state of the art?". Use case providers therefore have to evaluate their performances and their degree of adaptation to the industrial needs. To enable a precise and fair evaluation, all partners have participated to the definition of a set of metrics applicable to each tool and capable to measure its performances and quality. The subsections below list all requirements and their associated baselines

4.1 Common requirements

There are some requirements common to all the tools that need to be satisfied in order to be applied into an industrial context and they are listed in

Table 4.1: Common tool requirements

Requirement	**Priority/Character**	**Means of validation**
T1 The simulation speed shall be efficient.	Mandatory	Execution time of simulation should be comparable respect to state of the art, if present, otherwise should be faster that lower level abstraction model simulation tools.
T2 The simulation accuracy must be compatible with Use Case requirements	Mandatory	Tests on well-known models with validation against an actual experimental setup

4.2 Domain-specific requirements

4.2.1 Avionics domain

Tools coverage:

In the scope of the avionic domain, the following tools will be used and evaluated:

- UC CONTREP (CONTREX Eclipse Plug-in): Use case modelling; code generation; performance model generation for simulation.
- UC VIPPE: Native simulation; time, energy and power performance estimation.
- PoliMi MOST: Discrete optimization for DSE.

- Imperas OVP: VP-based simulation; time, energy and power performance estimation.

It has to be noted that VIPPE and OVP are used to perform system simulation at different abstraction levels. OVP simulation results can be used to validate the higher level native simulation results provided by VIPPE.

The following table includes the means of validation of the avionics domain requirements identified in D1.1.1 that are applicable to the CONTREX toolset.

Table 4.2: Tool requirements from the avionic domain

Requirement	**Priority/Character**	**Means of validation**
AVR-T1 CONTREX should support schedulability analysis.	.	It will be verified thatschedulability analysis tool results are the expected ones, by comparing them with the results obtained performing the schedulability analysis 'manually', using the same method(s) supported by the tool (as for instance, RMS or EDF). Both manual and automatic methods would use the same inputs, consisiting of the relevant information introduced in the model (periods, WCETs, deadlines, etc.)
AVR-T2 CONTREX should allow automatic code generation from model to generate performance models that enable system simulation.	Optional.	The tool's code generation rules will be reviewed and it will be checked if they are correctly applied when generating code from the demonstrator's model. In case this feature is actually provided by the CONTREX toolset, at least generation of code skeletons based on model's entities (such as components, classes, properties) would be expected, enabling the user to easily include the corresponding functional code. By way of example, if the code is to be generated in C language for a model that reflects the allocation of tasks or model components onto a real-time OS, the generation of independent C source files for each component and the presence of threads (either created using POSIX services or any other specific interface for performance models) would be expected.

AVR-T3 CONTREX shall support the detection and notification of possible violations of extra-functional properties by means of model-based system analyses/simulation.	Mandatory.	It will be verified that violations of extra-functiona properties are detected and notifed during system analysis and/or simulation performed by analysis and simulation tools. Constraints imposed to the demonstrator's model (such as execution deadlines or power consumption limits)must be guaranteed. In case they are violated during simulations, the simulator should notify them either in real-time or at the end of the excution. If necessary, specific modifications will be done on the demonstrator's model or source code in order to cause constraint violations during executions.
AVR-T4 CONTREX shall allow early estimation of resource usage/consumption.	Mandatory.	It will be verified that analysis/simulation tools provide high-level estimations on resource usage and consumption, and that these estimations are accurate enough according to the information included in the model. At least, estimations on time and power consumption
AVR-T5 CONTREX shall support the traceability from system requirements to models.	Mandatory.	It will be verified that a method to associate model elements with system requirements has been provided. This method might consist of: - a mechanism that allows to model requirements and then relate them with other model elements created in the successive development phases; - an annotation mechanism that allows to associate comments (including the requiremetn ID or text) to the model entities; or - any other similar mechanism. These associations between model entities and system requirements must be reflected in the demonstrator's model.

AVR-T6 CONTREX shall support the management of the items under configuration by using some kind of configuration management tool.	Mandatory.	It will be verified that the corresponding configuration management mechanisms are provided within the CONTREX development environment/toolset in order to perform version control of the models, the code generated and any other item generated/used by the CONTREX tools and that is subject to potential changes.
AVR-T7 CONTREX should allow the re-use of existing model libraries.	Optional.	It will be checked whether model libraries may be generated/reused using specific features of the modelling tools. For instance, it will be checked whether a model library describing a specific HW platform may be generated and then easily imported into different models.
AVR-T8 CONTREX shall assure model consistency by means of model validators and consistency checks.	Mandatory.	It will be verified that the modelling tools include model validators that perform the necessary checks in order to guarantee model consistency and correctness. Inconsistencies or errorsviolating the syntax or semantics of the corresponding meta-model will be introduced in the demonstrator's model in order to check whether theyare detected by the model validator.

4.2.2 Automotive domain

In the scope Automotive domain, the following tools will be used and evaluated:

- Docea Power. Power modelling tool, used for the SeCSoC platform.
- BBQLite. Low-cost sensor node run-time management firmware, used for the iNemo.
- N2sim: N2Sim augmentation for automotive telematics network scenario.

Table 4.3: Tool requirements from the automotive domain

Requirement	**Priority**	**Means of Validation**
AUT-T01 Docea Power shall interface to standard Iss and systemC simulation model trace for power state.	**Mandatory**	At design time. The system will be designd to fulfill the identified requirements. See (1) below.
AUT-T02 BBQLite shall	**Mandatory**	

provide an ANSI C implementation		
AUT-T03 A configuation configration tool for customizing the metric sensing infrastructure shall be available	**Optional**	
AUT-T04 BBQLite uses all power modes necessary for reducing power consumption. The quality of service is indeeed maximal to meet the power budget	**Mandatory**	Comparison with a hand-written optimized version of the code. See (2) below.
AUT-T05 The overhead of introducing run-time mangement should never exceed 10%maximum in time, power and memory footprint.	**Mandatory**	Calculation of performances, power and memory consumption (jobs, database) with and without GRM at simulation/run-time management. See (2) below.
AUT-T06 N2sim shall adopt standard protocol for communication between nodes and the cloud infrastructure	Optional	At design time. The system will be designd to fulfill the identified requirements. See (1) below.
AUT-T07 Crash processing services shall be ported on the cloud infrastructure	Mandatory	At design time. The system will be designd to fulfill the identified requirements. See (1) below.

The following list discusses in more detail the evaluation strategies listed in the table above.

1. Availability of the specific tools shall be guaranteed. The following criteria (where applicable) will be used for the evaluation:

    a. Ease of integration of design-time tools in the industrial flow. This criteria includes both the integration procedure in terms of IT infrastructure and in terms of the complexity/quality of the training necessary for designers to allow them efficiently using the tools.

    b. Ease of integration of run-time components into the existing application's firmware. This includes evaluating the possible changes required to the existing code and the quality of the documentation of the new modules.

    c. Configurability and usability will be evaluated, both for firmware modules and for the tools (e.g. the BBQLiteConf code generator). Some tools, such as the N2Sim simulator, require an application model to be provided as input. A crucial evaluation point is related to the training and development times

necessary to model the low-cost node and the key features of the application executed on it.

d. Quality of the results. This aspect is already covered by the evaluation approaches described in the other sections and related to modelling and to the general use-case requirements.

2. In some cases, evaluation of the quality of the tools is significantly related to the results they provide (in terms of quality of the resulting application) and the design-time effectiveness (e.g. shortening of the design time). Whenever possible, these aspects will be evaluated by

   a. Comparing the results obtained with the tools against existing firmware

   b. Comparing the design effort with past projects experiences.

4.2.3 Telecommunications domain

In the scope Telecommunication domain, the following tools will be used and evaluated:

- EDALab's extensions to SCNSL for network simulation
- EDALab's extensions to HIFSuite for virtual platform integration
- Docea Power: Power modelling tool

Table 4.4: Tool requirements from the telecommunications domain

Requirement	**Priority/Character**	**Means of validation**
TLC-T01 It must be possible to perform sufficiently realistic simulation of critical tasks in realistic network scenarios by using SCNSL.	**Some Optional and some Mandatory priorities of sub-requirements**	**Simulation of system operation in a realistic network scenario and verification of the correct behaviour of the critical tasks**
TLC-T02 Technology provider of CONTREX shall provide Intecs lab with the definition of the virtual platform representing the ZYNQ platform.	**Mandatory**	**Intecs lab will verify the possibility to automatically generate the definition of the virtual platform for ZYNQ starting from a description of its components**

TLC-T03 Technology provider of CONTREX shall provide to Intecs lab a power analysis environment to organize and trace power related data to ensure getting consistent power estimates	**Mandatory**	**Power simulation analysis using technology provider tools and methodologies.** The strategic aim is to acquire competences in using the combination of the simulation / trace generation / power analysis that are core CONTREX innovations, for incorporation into the Intecs engineering practices in new product development.
TLC-T04 Technology provider of CONTREX shall provide to Intecs lab a power analysis environment to make it easier to collect, reuse and share power related data	**Mandatory**	
TLC-T05 Technology provider of CONTREX shall provide to Intecs lab a power analysis environment to develop a holistic (covering all component types) and scalable (hierarchical) approach	**Mandatory**	
TLC-T06 Technology provider of CONTREX shall provide to Intecs lab a power analysis environment to make power estimation dependent on additional parameters/metrics (eg activity), i.e. not systematically rely on maximum power	**Mandatory**	
TLC-T07 Technology provider of CONTREX shall provide to Intecs lab a power analysis environment to improve power estimation accuracy	**Mandatory**	
TLC-T08 It must be possible to abstract the legacy VHDL IP blocks into SystemC/TLM to be integrated in the virtual platform	**Mandatory**	**Verification that the SystemC abstraction is consistent with the current system design**

5 Evaluation strategy of CONTREX approach

The objective of the task 5.3 “Evaluation of integration into industrial practice and flows” is the evaluation of the effectiveness of the entire design flow into the industrial state of the art development practices. This last task of the evaluation WP will verify that the CONTREX solution follows industrial standards and provides an estimation of the improvement that CONTREX flow brings compared to current design practices.

Main aspects to be evaluated:

1. The integrability in industrial flows

2. The portability into different supply-chain companies flows

3. Accuracy of the results

5.1 Avionics domain

In the current avionics development flow, the HW/SW partitioning decision and the specific platform characteristics and configuration are taken at an early stage of the cycle, and are usually based on the system architect’s experience and the usual practices in the development of similar systems. A set of HW and SW specific requirements are established before defining the system architecture, and then these developments evolve in parallel until the HW/SW integration phase. This may lead to problems when the system is deployed, as the platform may turn out to be not suitable for the SW generated (or vice-versa). If this is the case, it usually implies a SW re-design once it is finished, which is costly in terms of resources. In order to avoid this kind of problems, designers and developers rely exclusively on their previous experiences, and thus the design space is usually strongly limited. As a matter of fact, the decision of selecting a platform is usually made considering a very limited set of platforms that have been previously used with success in other projects. Moreover, the number of resources (processors, memories, buses) and their characteristics (processing frequencies, memory sizes, bus bandwidths) are usually oversized. Moreover, several platforms are employed in order to keep separated components with different criticalities, so their associated extra-functional properties can be guaranteed. This leads to unnecessary cost increases in case the system does not actually require more resources than those provided by a single platform.

Our main concern in CONTREX is to improve this flow by introducing extra stages of model-based analysis and simulation and DSE during the high-level system design (see Figure 5-1).Figure 5-1). This enhancement is expected to procure three main advantages:

- To select the most suitable platform (from a set of pre-defined platforms supported by the analysis and simulation tools) for the system in question, based on the information gathered during analysis and simulation.

- To select the most suitable system configuration (including the HW/SW partitioning scheme), based on the information gathered during the design space exploration.

- To avoid resource duplication and oversizing by checking, during the analysis and simulation phases, that the system’s extra-functional requirements and constraints are achieved.

In the case of the mixed-criticality systems, this will allow to define mixed-criticality systems and examine their performance in multi-core architectures (including commercial general-purpose platforms) in an early development phase, leading to a higher cost reduction.

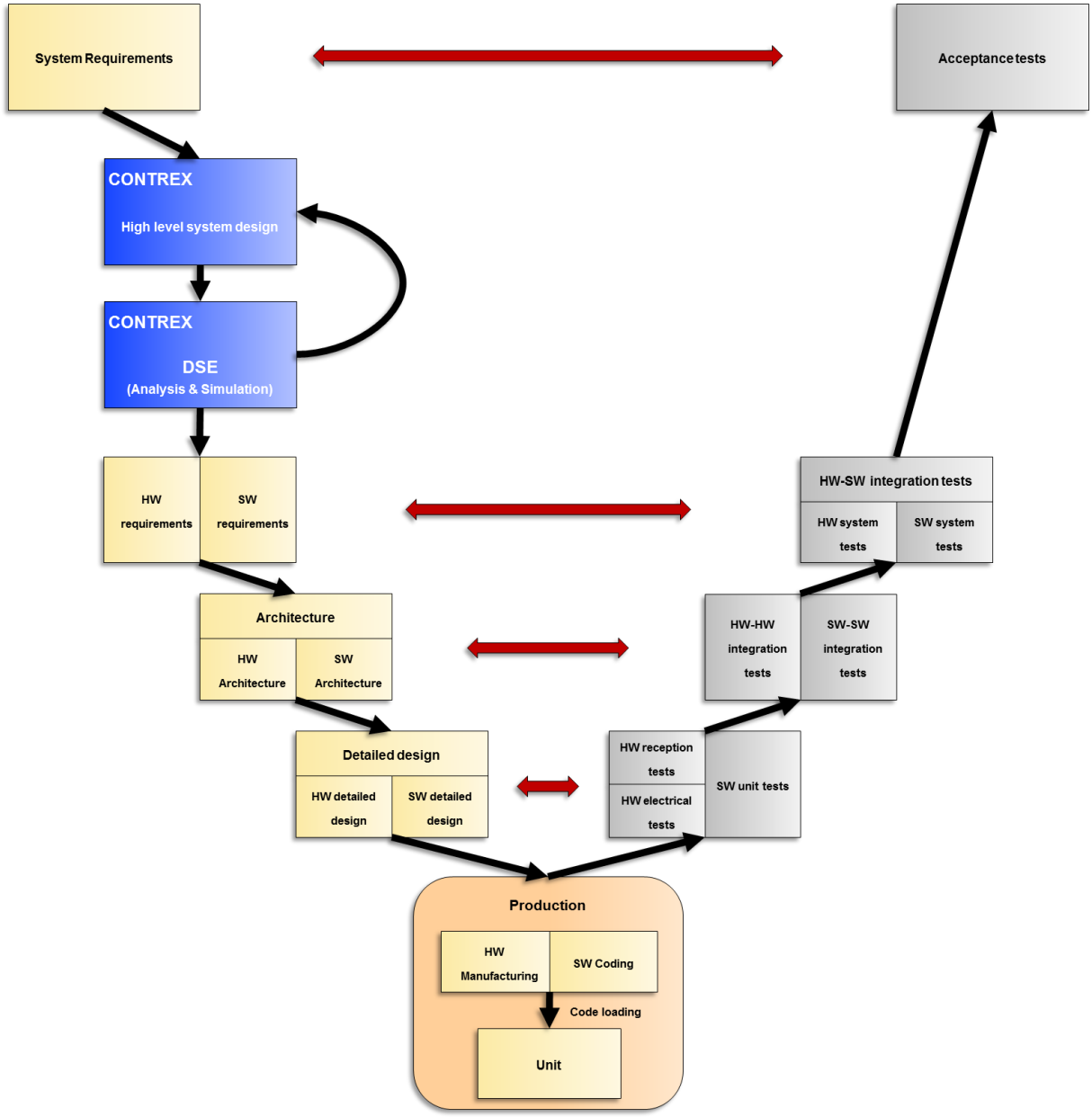


Figure 5-1: CONTREX-enhanced avionics development flow

The CONTREX workflow is being applied to the design and development of the avionics demonstrator (Use Case 1) for the purpose of evaluating the experience and results obtained by including the mentioned extra stages (blue boxes in Figure 5-1Figure 5-1) into the general avionics development flow. In order to make the CONTREX approach fit well into this flow and guarantee the introduction of the expected improvements, a set of requirements (applicable to the CONTREX modelling language, meta-model, methodology and tools) were

defined in D1.1.1 and reproduced, together with their corresponding means of validation, in the previous sections of this deliverable.

A three-step strategy will be followed for the evaluation of the CONTREX flow:

1. Evaluate to which extent the requirements on the CONTREX flow are met, using the means of validation specified for each requirement in previous sections. The level of coverage of these requirements will provide a measure of the integrability of the CONTREX approach into the avionics development flow.

While there are some optional requirements whose implementation would be only desirable, the 100% of the mandatory requirements should be covered by the CONTREX flow. A lower percentage will be considered acceptable if the reasons for not covering some requirement are conveniently justified or an appropriate alternative is provided.

2. Evaluate the accuracy of the results produced by the application of the CONTREX flow. The main results to be considered are:

    a. The estimations on extra-functional properties provided by the analyses and simulations performed during the DSE phase. The accuracy of these estimations will be measured by comparing them, to the extent possible, with the real values obtained from the executions in the real platform. In case of high-level native simulation, results can be also evaluated by comparison against results from VP-based simulation (which is usually more accurate).

    b. The outputs from the automatic DSE (putting it simply, the recommendations on the system's platform and the HW/SW configuration). As these outputs will strongly rely on the estimations provided by the analysis and simulation tools, the more accurate these estimations are the more reliable the outputs from the DSE can be considered.

3. Evaluate the resource savings that may be brought by the introduction of the CONTREX flow. These resource savings are expected to be the consequence of the usage of the results provided by it. Two kind of resources will be considered:

    a. Platform resources. These ones correspond basically to the physical components of the system and their specific characteristics. For instance, the number of SoCs, processors and memories composing the platform and their associated processing frequencies or memory sizes.

As previously said, one of the main advantages that is expected from CONTREX is the minimization, to the maximum possible extent (and without compromising the requirements and constraints on extra-functional properties), of resource duplication and oversizing. By means of accurate and fast system simulations, these estimations might become more precise and thus avoid extra costs on resources that are not being actually used, such as memory or processing capacity.

The improvement on resource usage estimations will be measured by comparing the estimations that are usually considered in current avionics development flow with the estimations obtained from the system simulations performed during CONTREX-specific phases, taking into account the average error measured for them (as explained in previous point).

b. Development time. CONTREX approach is also expected to enable the exploration of different design alternatives in a fast and easy manner. This exploration will provide information about which would be the optimum platform and HW/SW configuration according to a given criteria. In the case of the Use Case 1, the main objective of the DSE will be to minimize the power consumption while achieving all the requirements and constraints on extra-functional properties. The efficiency, in terms of time, of the CONTREX approach applied to the current avionics development flow will be measured from three different perspectives:

   i. In the first one, the time spent in the development of the Use Case 1 (including design, coding and deployment in the selected platform) using the current avionics development flow will be compared with the time spent using the CONTREX-enhanced flow (which includes DSE). In order to enable this exploration, several design alternatives, consisting basically of different HW/SW mappings, will be defined for the Use Case 1.

   ii. The second one will consist of comparing the time spent in exploring the design space automatically with the one that would be necessary for exploring it manually. For it, at least two of the design alternatives defined for Use Case 1 will be explored not only automatically but also manually.

   iii. Finally, the time spent in the development of the Use Case 1 using the CONTREX-enhanced avionics development flow will be compared with the total development time (using the current flow, without DSE) that would be spent in case a problem was detected in the HW-SW integration phase (for instance due to a design error, consisting on the selection of a wrong design alternative). For it, GMV's internal metrics regarding the cost of eliminating defects at different development phases will be used.

5.2 Automotive domain

The main changes related to the introduction of the CONTREX design tools into the current Cobra development flow concerns the following aspects:

Non-functional simulation. Energy and timing simulation of the node-level application developed on the iNemo platform by means of the POLIMI N2Sim simulator.

Monitoring infrastructure. Integration of the POLIMI non-functional property monitoring infrastructure into the application firmware.

Run-time management. This activity involves two components: the compile-time configuration tool BBQLiteConf and the run-time manager itself developed by POLIMI.

Cloud access. The switching from a dedicated, custom communication, storage and processing infrastructure to the EUTH Kura platform. This activity impacts on the development of application-specific software for the Kura pervasive platform and the on the cloud-side counterpart.

High-end node. The SeCSoC-based high end node for imaging purposes will only be subject to a preliminary evaluation in terms of performance and power consumption. The two main aspects to be evaluated will be related to the image-processing libraries provided by STM and power consumption models developed by STM and DOCEA.

The quality of the individual tools, models and methodologies with respect to several criteria has been covered in Sections 2, 3 and 4. In this section we outline the high-level criteria that will be adopted to evaluate the overall effectiveness of the CONTREX approach on the entire use-case scenario. For the sake of clarity, and for consistency w.r.t. the automotive use-case structure, the results to be considered for evaluation are summarized in the table below on a per-scenario basis.

Table 5.1: Validation of CONTREX design flow in the automotive use case

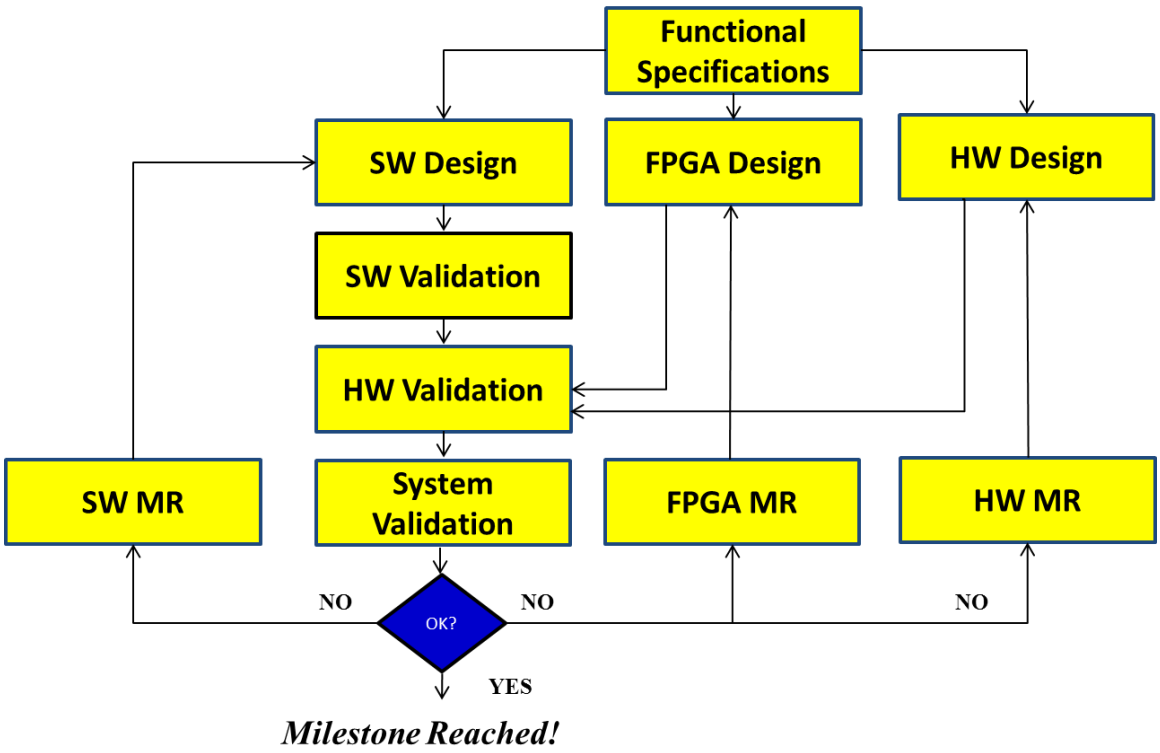
Scenario	Expected results	Means of validation
Device Installation	Average installation time reduction	Comparison of the installation time of the new device with average figures extracted from past installation reports. See note (1) below.
	Call rate reduction	Comparison against historical data. Note that collecting significant call rate data might require longer times than those allowed by the project duration, and thus the quantitative evaluation will only be considered preliminary. See note (1) below.
	False positive crash reports reduction	Comparison against historical data. See note (1) and (2) below.
Crash Management	Crash-to-call latency reduction	Comparison with historical quality-of-service data. See note (2) below.
	Cost reduction	Evaluation of the expected cost reduction as a consequence of false positive crashes and the improved sensing quality of the sensor nodes.
Key-off services	New business opportunities	New contacts and/or preliminary agreements with insurance companies requiring new generation key-off services.
B2B Services	Scalability	Provide evidence of the scalability opportunities offered by the cloud-based solution.
	Cost reduction	Comparison of the expected cost growth of the current ad-hoc solution with the cloud-based approach.
	Employee/Customer	Preliminary estimation of the trend of this

	ratio reduction	figure.
	New business opportunities	New contacts and/or preliminary agreements with new stakeholders.
Notes. (1) The installation of a limited number of devices is foreseen before the end of the project. Due to the long industrialization times, it is not feasible to envisage volume installations. (2) Critical installation situations and crash events can be forcibly reproduced and used for pre-evaluation, before in-field validation.		

5.3 Telecommunication domain

The aim of Intecs is to exploit the CONTREX tools and methodologies in order to improve its current products design flow.

Fehler! Verweisquelle konnte nicht gefunden werden. shows the current Intecs product design flow.



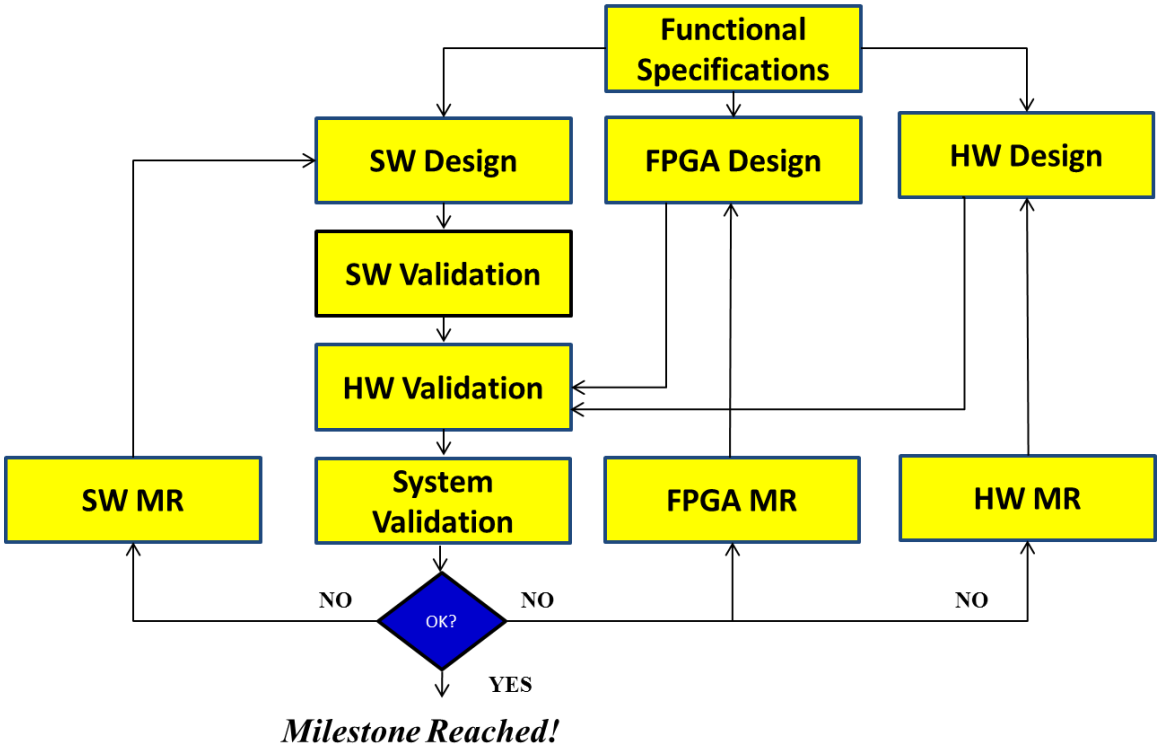


Figure 5-2: Current Intecs Design flow

Currently, Software and Hardware/FPGA labs start from the customer functional specifications and begin the development phases.

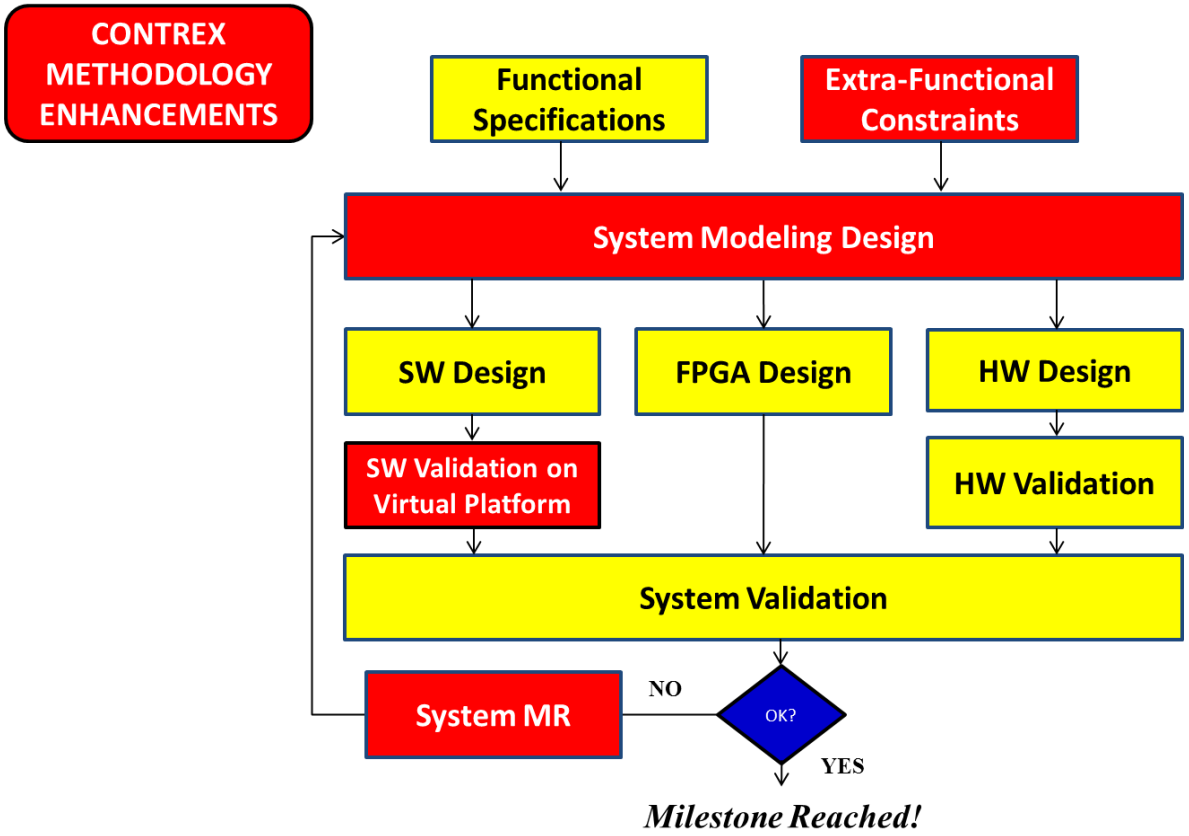
The Hardware validation can be performed just at the end of both Software and Hardware/FPGA development.

This produces some drawbacks:

- System Validation phase starts very late, at the end of the integration phase among Software, Hardware and FPGA development;
- Especially on the early stage of system validation, testing highlights a huge amount of bugs and specifications not respected (both functional and extra-functional ones). This produces a significant number of so-called Modification Requests (MR), used to trace any problem in the system.
- Very often, due to the lack of a simulation environment, system validation highlights problems in terms of power consumption or thermal dissipation. Very often, even if all the functional specifications were achieved, the time-to-market has been increased due to energy consumption that is either unacceptably high or in any case not compliant with customer expectations.
- The whole design flow becomes very inefficient as system complexity increases.

For all the reasons mentioned above, Intecs expects to improve the efficiency of its design flow by exploiting the CONTREX tools and methodologies with the aim to reduce the time-to-market of future products.

Figure 5-3Figure 5-3 shows the enhancements that Intecs expects to achieve within the CONTREX project.



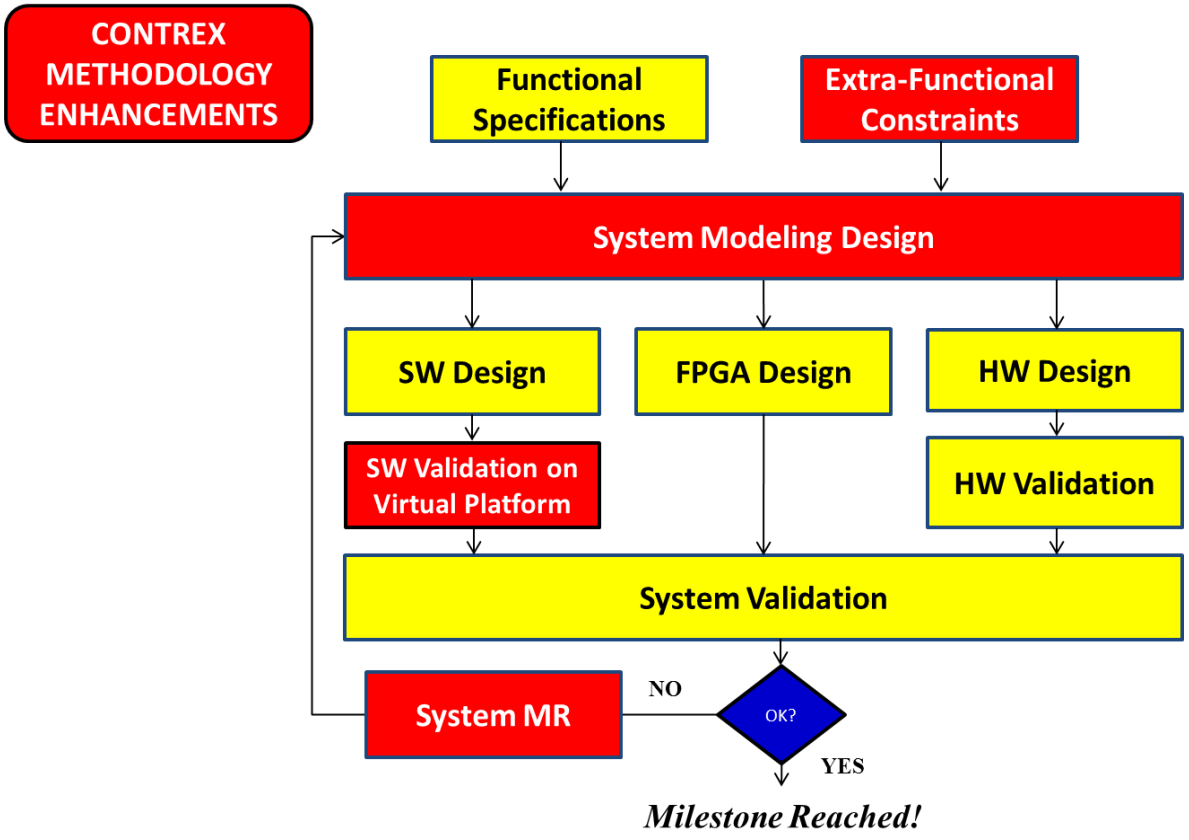


Figure 5-3: Expected CONTREX-Enhanced Design flow

As depicted in the previous figure, the enhancements expected in the design flow are the following:

- Introduction of a System Modelling Layer Design, in order introduce also the Extra-Functional constraints (Power and Thermal) in the early stage of the design phase. This would lead the Intecs Telecom lab to verify all design needs before starting with Software and Hardware/FPGA development, avoiding huge amounts of problems during the System Validation phase.

- Introduction of a Virtual Platform environment in order to start the Software application tests before having availability of the Hardware board. This would lead to a significant reduction of the time-to-market because Software and Hardware validation phases could start in parallel.

- As a consequence, Intecs Telecom lab expects to reduce the number of Modification Requests, due to the tests performed at a System Modelling level. Software, Hardware and FPGA MR would be replaced by the concept of System MR, leading to a modification at a System Modelling Layer.

The CONTREX enhancements can be fully integrated in the current Intecs Telecom labs development processes. They provide also the possibility of incremental enhancement of the processes. For example, the system modelling layer already brings benefits independently from the virtual platform technology. Conversely, the virtual platform technology provides benefits on its own with regard to early validation, independently from the application modelling techniques introduced by CONTREX.

This means that the CONTREX innovations provide a modular, incremental path to an improved product development lifecycle in the Intecs Telecom Lab. Different product development processes can be configured to include some or all of the CONTREX enhancements, depending on the particular demands of the product profile.

In order to be able to perform as complete an evaluation as complete as possible of the efficacy and accuracy of the elements of the CONTREX approach, Intecs plans to follow the modelling flow depicted in Figure 5-4Figure 5-4, coordinating contributions of several technology providers together with the mainstream Intecs implementation and evaluation activities.

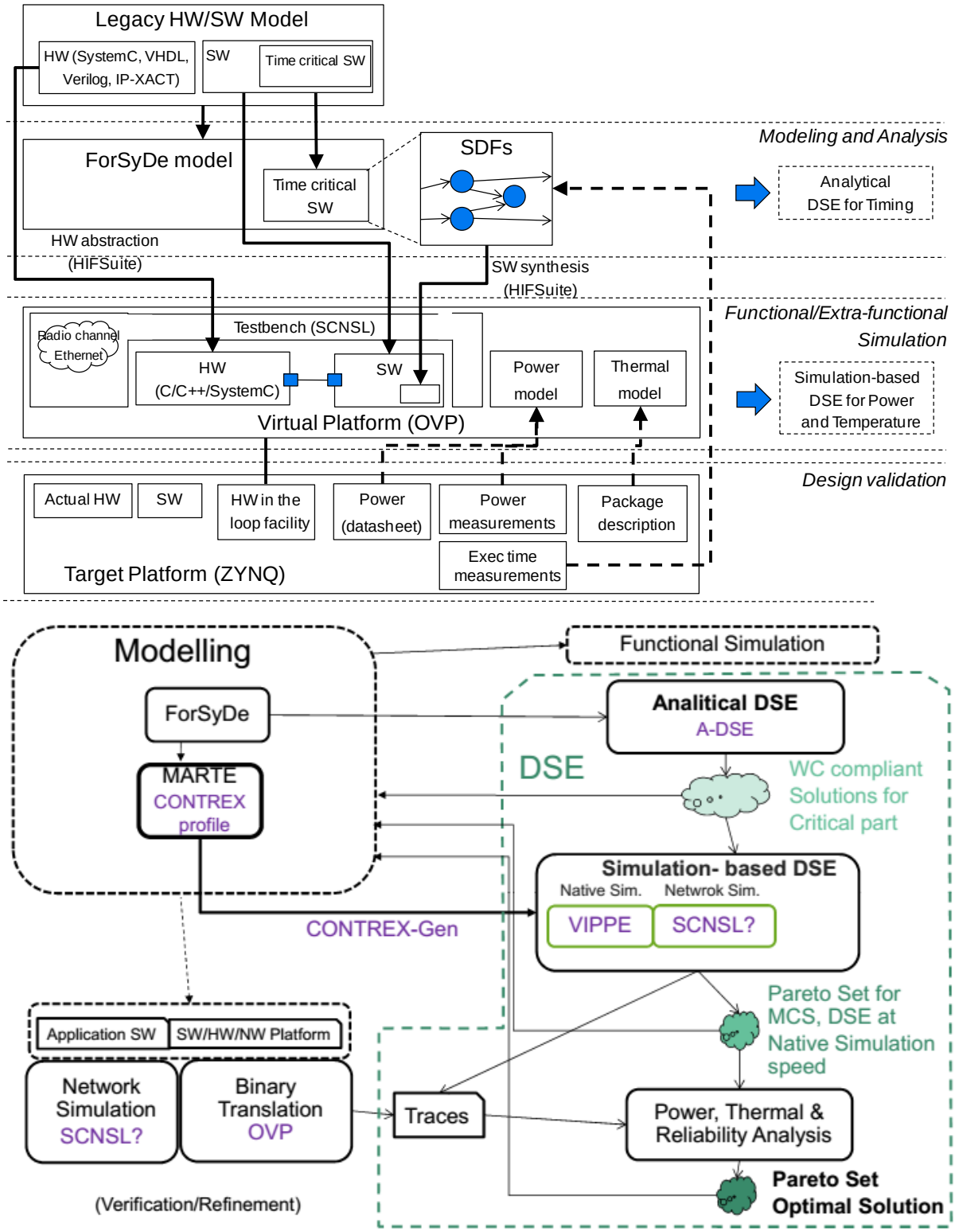


Figure 5-4: Modelling flow for UC3

One of the most important aspects of this use case is the use of a pre-existing system to be improved. Because of this, most of the models come from legacy components.

The most time critical software components are ported to ForSyDe for schedulability analysis. Intecs is working with KTH in order to model the critical areas of the Telecom application software, with the intention of producing ForSyDe models sufficiently expressive to enable

the subsequent phase of analytical Design Space Exploration with the relevant ForSyDe analysis tools / techniques. KTH is also investigating the possibility of generating code from the Use Case 3 ForSyDe models for implementation on predictable platforms as part of their own research.

The main result of the analytical DSE performed by Intecs and KTH is expected to be, in particular, design solutions that are compliant with time-criticality requirements of the application. In addition, other possible improvements are expected in terms of architecture and overall efficiency. For example, Intecs and KTH will collaborate in exploring different approaches to migration from single core to multi-core application architectures.

The University of Cantabria (UC) has been investigating the automatic conversion of ForSyDe into UML/MARTE; therefore the ForSyDe models produced by Intecs can be used by UC as a further testbench to evaluate its conversion tool.

As part of their research, KTH and UC will compile the ForSyDe models produced by Intecs application models into executable models by relying on the ForSyDe-SystemC library.

Even if ForSyDe models can be executed through SystemC, a full OVP-based simulation will be also exploited. ForSyDe models will be translated to SW components either manually or by using HIFSuite. Legacy HW components (e.g., written in VHDL) will be integrated into the OVP scenario by using HIFSuite.

The ZYNQ platform for simulation in the OVP environment will be provided by OFFIS and EDALab. One goal of the Intecs simulation activity on the OVP will be power and thermal analysis, as discussed in the following Section. The SystemC Network Simulation Library (SCNSL) will be used to reproduce a network scenario to be used as testbench in the simulation.

The simulation runs performed by **Intecs** on the Open Virtual Platform will generate the traces (using the OVP extensions provided by **OFFIS**) that will serve as input to the tools provided by **Docea**/**OFFIS** for (offline) analysis and optimization of thermal and power related properties.

In order to do that, the following evaluation scenarios are envisioned as a test bench.

1. FIRST EVALUATION SCENARIO: Porting of current SW to ARM and Power measurements on System Controller & FPGA Power estimation

The existing source code will be ported to the Xilinx Zynq platform **modelled on the Open Virtual Platform** (the SW part is ported to the ARM dual core system running Linux in SMP mode).

Since the first scenario might not beat the existing system in terms of total power consumption (because the Xilinx Zynq platform might not be fully utilized) a second conceptual case study will evaluated in next section.

2. SECONDEVALUATION SCENARIO: Integration of multiple Ethernet over Radio channels in a single SoC (Xilinx Zynq)

A second case study, still performed on the **Open Virtual Platform**, is the integration of multiple Ethernet over Radio channels in a single SoC (Xilinx Zynq).This second scenario will be performed at a more conceptual level but shall nevertheless fully exploit the Xilinx Zynq platform resources, to demonstrate that the possible increased power consumption is

more than compensated by the enhanced transmission functionality (support of multiple modems).

The total power consumption of the 2nd conceptual multi modem on chip design can be evaluated based on the estimates obtained from the 1st scenario.

After the modelling phase is ended, Intecs intends to port its application **to a real Zynq board**, in order to evaluate the reliability of:

- the Virtual Platform models of Zynq on OVP;
- the Network Simulation environments (SCNL) implementation;
- power traces analysis results.

6 References

[1] "Description of Work". CONTREX –Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties,FP7-ICT-2013- 10 (611146), 2013.

[2] D.1.2.1 “Definition of industrial use cases”