Dissemination Report (Intermediate)

Public

FP7-ICT-2013- 10 (611146) **CONTREX**

Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties

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WP6	**D6.3.3**	**ECSI**

Dissemination Report (Intermediate)

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ED.	REV.	DATE	PAGES	REASON FOR CHANGES
AM	0.1	2015-04-03	10	Initial version
IS	0.2	2015-04-17	18	Added KTH contributions
SK	0.3	2015-04-19	18	Added DOCEA contributions
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FH	0.5	2015-04-22	20	Added UC contributions
AG	0.7	2015-04-22	20	Added IX contributions
AM	1.0	2015-05-08	21	Final version

Contents

1 Introduction

This document summarizes all dissemination activities that were undertaken by the CONTREX project consortium as a whole and by each individual partner of the consortium in the period between 10-18 month of project execution.

In this period cooperation between relevant R&D projects in FP7 and CATRENE were strengthened by specific common activities:

- With the OpenES project internal presentations and preparation of the DAC Workshop on System to Silicon Performance Modeling and Analysis.
- With the Mixed-Criticality Cluster: preparation of common booth at the ARTEMIS Co-Summit and preparation of the Special Session at the FDL Conference

These activities created a very good basis for collaboration with other projects and for establishing relations with the community (research partners and potential industrial customers) of the CONTREX results.

2 Consortium-Level Dissemination Activities

2.1 MCC Workshop – Brussels, Belgium – July 2, 2014

The European mixed-criticality cluster consisting of the three EU FP7 projects CONTREX, DREAMS and PROXIMA organised an internal workshop that took place on July 2nd in Brussels. The workshop aimed the mutual technical understanding of planned work in the projects as well as to present first research results in the projects, to identify synergies in future standardisation activities and to foster the collaboration in between the cluster.

All three projects contributed to the workshop with 12 technical presentations and a total of about 50 attendees. CONTREX contributed with the following two presentations:

- Modelling of Distributed Embedded Mixed-Critical Systems
- Analysis of extra-functional properties power, temperature, and degradation in MCS

Target audience: Universität Siegen (USIEGEN), IKERLAN S. COOP (IKL), Thales SA (TRT), Office National d'Études et de Recherches Aérospatiales (ONERA), RealTime-At-Work (RTAW), TTTech Computertechnik AG (TTT), Technische Universität Kaiserslautern (TUKL), Fortiss GmbH (FORTISS), Stiftelsen SINTEF (SINTEF), Alstom Renovables España S.L. (ALSTOM), STMicroelectronics (ST), Virtual Open Systems (VOSYS),

Technological Educational Institute of Crete (TEI), Polytechnic University of Valencia (UPV), Fent Innovative Software Solutions (FENTISS), TÜV Rheinland Industrie Service GmbH (TUV), Airbus, Airbus Defence & Space, Barcelona Supercomputing Center, Aeroflex Gaisler, Ikerlan, Infineon, INRIA, RAPITA Systems, Sysgo, Universita degli Studi di Padova, University of York

Participation: 50 participants from 3 project consortia

Follow-up actions: common MCC website creation, submission of proposal of a joint Special Session at FDL, joint dissemination actions (e.g. ARTEMIS Co-Summit

2.2 DATE 2015 Tutorial

The power of Power in future wireless smart systems for the Internet of Things

Grenoble
ALPEXPO-ALPES Congres
Monday 9 March, 2015
14:30-18:00
http://www.date-conference.com/conference/tutorial-m08/form

In the future, objects and people will be almost permanently connected and exchanging information in the so-called Internet of Things (IoT). While the potential influence of IoT in our daily life is enormous, there are major challenges related to its energy sustainability. Also in the healthcare domain, progress in microelectronics has enabled the miniaturization of data processing elements, radio transceivers and sensors for medical applications. However, the inherent resource-constrained nature of these systems, coupled with the specific operating conditions and the stringent autonomy requirements pose important design challenges. The evolution of battery energy density is below the curve of Moore's law thus making power consumption the limiting factor of next-generation smart systems. Furthermore, technology allows integrating various types of energy harvesting devices, which are able to scavenge energy from the environment thus potentially compensating the increased gap between the energy demand and its availability.
This tutorial addresses all these issues involving energy management in autonomous wireless devices from a novel perspective. As a matter of fact, while the analysis and the optimization of how energy is consumed in electronic systems has been the subject of many studies, a lot of misconceptions are still around when it comes to how optimally generate, store, convert and distribute the energy available in a system that incorporates energy generation and storage devices.

The tutorial will cover the following key topics:
1) Architecture of wireless autonomous smart systems and design challenges
2) Energy storage devices: background and non-idealities, models and design guidelines, conversion issues
3) Energy harvesting techniques and architectures for energy neutral systems
4) Power management policies and protocols for autonomous objects
5) Modeling and simulation techniques
6) Trends for future wireless smart systems

The presentations will report results from SMAC and CONTREX European projects and will be accompanied by actual case studies, showing how the presented concepts support the design and verification of wireless autonomous smart systems.

The tutorial is targeted towards students and pratictioners belonging to both academia and industry and concerned with design of advanced wireless embedded systems (e.g., wearables, smart metering, body sensor networks, etc).

Speakers:
Massimo Poncino, Politecnico di Torino, Italy
Davide Quaglia, EDALab s.r.l., Italy
Alain Pegatoquet, LEAT/University of Nice Sophia Antipolis, France

2.3 ARTEMIS Co-Summit - Berlin, Germany – March 2015

The seventh edition of the annual Co-summit "Smart Industry: impact of software innovation" took place at the Berlin Congress Center on 10/11 of March 2015. The Co-summit was jointly organised by ITEA, the EUREKA Cluster on Software-intensive Systems & Services and by ARTEMIS Industry Association, the association for actors in Embedded & Cyber-Physical Systems within Europe.
Over two days a diversity of projects, presentations and discussions demonstrated the central and crucial role played by ITEA and ARTEMIS projects in the creation of new, smart manufacturing and processing. In her keynote address, Jutta Schneider, Director of eDrive and Software Technologies at Daimler AG, underlined the importance of "software innovation as a key driver", a view that was resoundingly echoed by other prominent speakers from the German government, the European Commission and industry. During the panel discussion on the Co-summit theme, TNO's Egbert-Jan Sol suggested that "it is not simply software innovation but also business innovation and social innovation" that are keys to the evolutionary process that is revolutionising industry. Importantly, Thomas Lagerberg of ABB put the question: "We have all these big data and connectivity but it is important to ask what's in it for me, how can I make money out of it? We have to demonstrate the benefits to people."

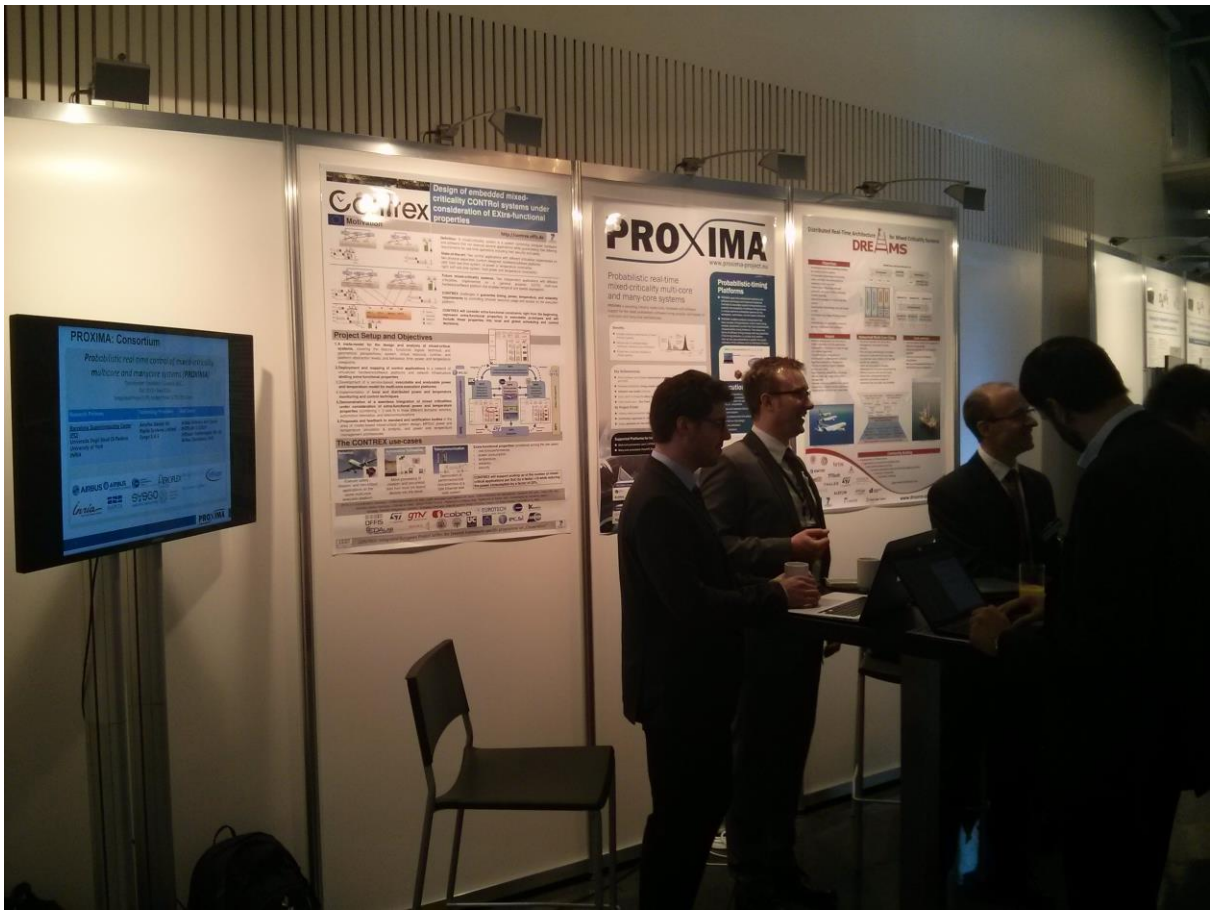
Examples of precisely such benefits were being displayed all around the exhibition floor: ARTEMIS and ITEA projects that not only captured the imagination but actually showed to more than 700 visitors and participants the tangible impact of their work. Like the R5-COP autonomous WALL•E-looking robot wandering around the exhibition floor, an example of a smart solution for dirty and dangerous jobs, or the BaaS project leaders in their hardhats and hazard warning vests that attracted interest in the use of novel value-added services and applications for smart commercial buildings – both winners of the Exhibition Award.

Speakers corners offered insight into smart industry trends, such as the future of automated driving with a focus on secure connectivity and the role of Cyber-Physical Systems as a key technology in the connectivity. Or the dilemma of financing healthcare in which Philips believes that by cleverly linking Cyber-Physical Systems the costs of realising requirements for the healthcare system chain can be reduced. Speakers from as far as Canada and South Africa underlined the global dimension of the Co-summit and the European programmes.

The CONTREX project participated in this event together with the other Mixed Criticality Cluster projects DREAMS and PROXIMA. On one hand, there was a joint MCC exhibition booth to promote the Mixed Criticality Cluster and the project topics. On the other hand, the cluster organized a Speakers' Corner with presentations and discussions on mixed-criticality systems.

Target audience: industry and academia involved in ARTEMIS/ITEA Programmes

2.4 MCC Exhibition Booth



2.5 MCC Speakers Corner

The speakers corner with the title “Towards Platforms for Mixed-Criticality Systems” on mixed-criticality systems was held on 10 March 2015 with the following agenda:

14:00 - 16:00 Towards Platforms for Mixed-Criticality Systems

14:00 - 14:05 Mixed-Criticality Systems and Research Challenges

14:05 - 14:15 Vision of the European Commission

Multi-Core Platforms for Mixed-Criticality Systems

14:15 - 14:30 DREAMS - EC FP7

14:30 - 14:45 PROXIMA - EC FP7

14:45 - 15:00 EMC2 - ARTEMIS

15:00 - 15:15 P-SOCRATES - EC FP7

Development Methodologies for Mixed-Criticality Systems

15:15 - 15:30 CRYSTAL - ARTEMIS

15:30 - 15:45 CONTREX - EC FP7

15:45 - 16:00 MBAT - ARTEMIS

2.6 2nd DAC Workshop: System to Silicon Performance Modeling and Analysis

This is the second workshop organized jointly by CONTREX and OpenES projects to create the momentum in the community around the aspects of modelling of extra-functional properties. The objective for both projects is to exchange information on advances and results, but also to present them to the industry in general sense. This is why the workshop is organized in the context of the major international conference DAC (Design Automation Conference) to gain exposure to major industry players.

This year also the presentations in the workshop will be given by several partners otside of the project consortia including Intel, Xilinx, ARM, Cadence, IMEC, IROC, Toshiba and several renowned research partners.

Workshop Program		
9:00	**Intro**	**Welcome & Agenda** *Adam Morawiec (ECSI)*
9:05	**Keynote**	**An Accurate Simulation Framework for Thermal Explorations and Optimizations** *William Fornaciari (PoliMi, Italy)*
9:50	**Session 1**	**System-Level Design for Reliability** Organizers: *Andreas Herkersdorf (TU München, Germany), Jürgen Becker (KIT Karlsruhe, Germany)* Abstract: Reliability is a system-level concern, both from the hardware/software architecture as well as design method perspectives. Advanced nanometer CMOS technologies are known to be increasingly vulnerable for radiation induced sporadic soft-errors, device aging and various forms of manufacturing and environmental variations. Another source of reliability exposures for today's and future Systems-on-Chip (SoC) solutions is their inherent complexity, expressed either in Billions of transistors, number of IP cores integrated, and the variety of huge functionality implemented on a single SoC. Today, it is already practically infeasible to validate such SoCs down to clock cycle accuracy under various representative workload scenarios. Both, feature size and complexity induced challenges cannot be addressed at individual, specific abstraction layers with acceptable quality and cost. Senior university and industry researchers from the US and Europe will share their perspectives on crucial design aspects of today's and future embedded and cyber physical systems. Topics span from dependable NoC communication virtualization on MPSoC, to self-aware Cyber Physical Systems-on-Chip, to high-throughput database query acceleration on reconfigurable FPGAs with High-Level Synthesis, to reliability management of 3D stacked wireless baseband SoCs.
9:50	**1.1**	**A Cross Layer Approach for Efficient Reliability Management in 3D Stacked Wireless Baseband SoCs** *Norbert Wehn (Microelectronic System Design Research Group, University of Kaiserslautern, Germany)*
10:15	**1.2**	**Using Roofline Models to Analyze the Performance of Realistic Key Value Store Implementations on FPGAs with High Level Synthesis** *Kees Vissers and Michaela Blott (Xilinx, USA and Ireland)*
10:40	**1.3**	**CyberPhysical-System-On-Chip (CPSoC): A Self-Aware SoC Platform for Cross-Layer Reliability**

		Nikil Dutt (Center for Embedded and CyberPhysical Systems, UC Irvine)
11:05		Coffee Break
11:20	**1.4**	**Intel Euro Labs Presentation (TBC)** *Enno Lübbers, Intel Euro Labs, München, Germany*
11:45	**1.5**	**Enabling Dependable MPSoC Task Migration with On-Chip Interconnect Virtualization** *Andreas Herkersdorf (Integrated Systems Lab, Technische Universität München, Germany)*
12:10	**1.6**	**Dynamic Migration and Performance Optimization of Deterministic Applications Across Platform Components Using Intel® CoFluent™ Studio** *Jérôme Lemaitre, Rocco Le Moigne (Intel Corporation SAS, France)*
12:35		Lunch Break
13:15	**Keynote**	**Towards Parallel Simulation of Multi-Domain System Models** *Rainer Dömer, UC Irvine, USA*
14:00	**Session 2**	**Tools and Methods for Power and Temperature Modeling and Analysis** Organizers: *Kim Grüttner (OFFIS, Germany), Domenik Helms (OFFIS, Germany) Laurent Maillet-Contoz (STMicroelectronics, France)* Abstract: With the predicted device, core and multicore scaling, the dark silicon hypothesis predicts the end of multicore scaling, regardless of chip organization and topology, due to power or energy density limitations. For this reason, future system engineers should be able to address power and thermal management as soon as possible in the design flow. Introduction of power and temperature management cannot be done at a single abstraction layer, but must be taken into consideration from the operating system, early system-level models, down to the integration of RTL IP components. For this reason, power and temperature properties need to be modelled across all abstraction layers, because they can strongly affect the products overall quality of service or even cause the system to fail meeting its real-time and safety requirements. In this session will discuss breakthrough academic and industrial solutions to control power consumption and heat dissipation at design and run-time. Furthermore, this session will discuss proposed extensions of existing industrial standards and their implications on commercial tool support. The addressed topics are: operating system support for fine-grained system-level energy analysis through orchestration of energy measurements at hardware level; the extensions of IP-XACT and UPF industry standards to support a seamless ESL to RTL low power design methodology; the extension of IP-XACT with verification features including portable stimuli vectors to enable performance and power closure of complex SoCs; tools for architectural level power and thermal modeling; and a new thermal constrained run-time management called “Thermal Safe Power”.
14:00	**2.1**	**The FIGAROS Operating System Kernel for Fine-Grained System-Level Energy Analysis** *Timo Hönig, Heiko Janker, Wolfgang Schröder-Preikschat (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany)*
14:25	**2.2**	**Extending IP-XACT and UPF to Support ESL to RTL Low Power Design Methodology** *Emmanuel Vaumorin, Grégoire Avot (Magillem Design Services; France), Hend Affes, Michel Auguin, Alain Pégatoquet, François Verdier (Univ. Nice Sophia Antipolis, France)*
14:50		Coffee Break
15:05	**2.3**	**IP Configuration for the Right Balance Between Required Performance and Power** *Nick Heaton (Cadence Design Systems, USA), Simon Rance (ARM, UK)*
15:30	**2.4**	**The Use of High Level IP Power Models Across System Analysis Environments and Teams** *Sylvian Kaiser (Docea Power, France)*
15:55	**2.5**	**Thermal-Aware Power Budgeting for Dark Silicon Chips** *Santiago Pagani, Muhammad Shafique (Karlsruhe Institute of Technology,*

		Germany), Jian-Jia Cheny, Jörg Henkel (TU Dortmund, Germany)
16:20	**Session 3**	**Ageing and Variation Prediction from Transistor to RT Level** Organizers: *Christoph Sohrmann & Roland Jancke (Fraunhofer Institute for Integrated Circuits IIS, Germany)* Abstract: Even in safety-critical areas such as Automotive, Aviation, Medical, and Industrial the demand for applications having highest performance, lowest energy consumption, and smallest dimensions together with extended service life grows rapidly. Combinations of these requirements can only be provided by extremely scaled technologies. Such safety-critical applications do not tolerate device failure. However, devices from advanced technology nodes are generally more susceptible to parametric deviations, either from process variations, parametric drift over lifetime or a combination thereof. The correct prediction of parametric deviations is similarly important as making them accessible on higher abstraction levels. The focus of this session are thus models and formats which abstract detailed knowledge about parameter variations and reliability from the device level to the circuit or RT level. The solutions presented will enable the designer to take these effects into account early in the design phase and ensure to meet specifications over the entire lifetime and for all application conditions.
16:20	**3.1**	**Impact of Time-dependent Variability on the Yield and Performance of 6T SRAM Cells in an Advanced HK/MG Technology** *Pieter Weckx, Ben Kaczer, Praveen Raghavan, Francky Catthoor, Guido Groeseneken (IMEC, Belgium)*
16:45	**3.2**	**Facilitating Cross-Layer Reliability Management through Universal Reliability Information Exchange** *Enrico Costenaro[1], Domenik Helms[2], Nematollah Bidokhti[3], Adrian Evans[1], Maximilian Glorieux[1] and Dan Alexandrescu[1] ([1]IROC Technologies, France; [2]OFFIS, Germany; [3]OCZ Toshiba, USA)*
17:10	**3.3**	**Statistical Timing Methodology for Low-Power and Multi-Voltage Designs** *Kerim Kalafala, Natesan Venkateswaran, Stephen Shuma, Vladimir Zolotov, Eric A Foreman (IBM Thomas J. Watson Research Center, USA)*
17:35	**3.4**	**Reliability-Driven Analog Circuit Design using gm/Id Method and Cross Layer Modelling of Aging** *Steffen Paul, Nico Hellwege, Nils Heidmann, Dagmar Peters-Drolshagen (Institute of Electrodynamics and Microelectronics, ITEM, University Bremen, Germany)*
18:00		**Concluding Remarks & Closing** *Adam Morawiec (ECSI)*

Expected Audience: large representation of world-wide system and microelectronics industry

2.7 Dissemination Material and Means

2.7.1 Web site updates

The project web site is available at: https://contrex.offis.de

2.7.2 Poster

2.7.2.1 CONTREX Project Overview Poster

A dedicated poster has been developed to present it at events and booths.

3 Partner-Level Dissemination Activities

3.1 OFFIS E.V.

3.1.1 Publications

2015

- Sören Schreiner, Kim Grüttner, Sven Rosinger and Wolfgang Nebel. „**Ein Verfahren zur Bestimmung eines Powermodells von Xilinx MicroBlaze MPSoCs zur Verwendung in Virtuellen Plattformen“** In 18. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2015). March 2015.

2014

- Domenik Helms and Kim Grüttner and Reef Eilers and Malte Metzdorf and Kai Hylla and Frank Poppen and Wolfgang Nebel**. “Considering Variation and Aging in a Full Chip Design Methodology at System Level”.** The 2014 Electronic System Level Synthesis Conference (ESLsyn'14), May 31- Jun 01 2014, San Francisco, CA, USA.

- Daniel Lorenz and Kim Grüttner and Wolfgang Nebel. **„Data- and State-Dependent Power Characterisation and Simulation of Black-Box RTL IP Components at System-Level“.** 17th Euromicro Conference on Digital Systems Design (DSD 2014).

- Gregor Nitsche and Kim Grüttner and Wolfgang Nebel. “**Towards Satisfaction Checking of Power Contracts in Uppaal**”. Forum on Specification and Design Languages 2014, October 2014, Munich, Germany.

3.1.2 Presentations at Conferences / Workshops

2015

- Kim Grüttner. “Empowering mixed-critical system engineers in the dark silicon era: Towards power, temperature and aging analysis of heterogeneous MPSoCs at system-level”. Keynote at 1st Workshop on Model-Implementation Fidelity (MiFi) at DATE'15.

- Kim Grüttner. “**Towards Platforms for Mixed-Criticality Systems”**. MCC Speakers Corner at ARTEMIS/ITEA Co-Summit 2015, March 2015, Berlin, Germany.

- Kim Grüttner. “Towards power, temperature and aging analysis and estimation for SoCs at system-level”. Workshop MCS: Integration of mixed-criticality subsystems on multi-core and manycore processors at HiPEAC Conference, January 2015, Amsterdam, Netherlands.

3.1.3 Exhibitions and Demonstrations

- ARTEMIS/ITEA Co-Summit 2015: **Mixed Criticality Project Cluster Exhibition Booth**, March 2015, Berlin.

3.1.4 Other dissemination activities

2014

- Face-to-Face meeting "Roadmap for SystemC Standardisation" at DVCon Europe, October 2014, Munich, Germany.
- Face-to-Face meeting "Roadmap for Accellera CCI-WG" at DVCon Europe, October 2014, Munich, Germany.
- Special Session "Mixed-Criticality System Design, Implementation and Analysis". At EUROMICRO DSD/SEAA 2014. August 2014, Verona, Italy. Special Session Chairs: Kim Grüttner and Eugenio Villar.

3.2 STMICROELECTRONICS, ST-I

There were no specific dissemination activities reported in this period.

3.3 GMV AEROSPACE AND DEFENCE SA UNIPERSONAL

There were no specific dissemination activities reported in this period.

3.4 COBRA TELEMATICS

There were no specific dissemination activities reported in this period.

3.5 EUROTECH

3.5.1 Publications

"Shunting data", Rail Professional Magazine, 9/9/2014

"Kura - A Gateway for the Internet of Things", Eclipse Newsletter, February 2014

Intel and EUROTECH, UBM, An IoT Blueprint, "Connecting Business with Machines in the Cloud-Based World of IoT", February, 2015.

Oracle, Eurotech, Hitachi, Oracle Java Embedded Whitepapers, "Eurotech M2M Technical Building Blocks Focus on a Multi-Service Gateway Approach and Standards-Compliant Software Elements", 2014.

"Kura - A Gateway for the Internet of Things", Eclipse Newsletter, February 2014.

3.5.2 Presentations at Conferences / Workshops

"Shoot-A-Pi with Eclipse Kura", EclipseCON 2015, San Francisco, March, 2015.

"Device Management for OSGi IoT Gateways", EclipseCON 2015, San Francisco, March, 2015.

"M2M/IoT Gateway: reducing the distance between embedded and enterprise technologies", EclipseCON, Ludwigsburg, October, 2014.

Eurotech chaired the Panel Discussion "Next Generation Telematics through Advanced Connectivity" at Automotive Telematics 2014 in Berlin.

"Creating a Java IoT Gateway", JavaOne, San Francisco, September, 2014.

3.5.3 Exhibitions and Demonstrations

IoT Evolution Conference & Expo - Battle of the Platforms – Las Vegas, August 2014 – Eurotech received the award "Best Vertical Implementation" of M2M solutions.

Participation as a technology provider in the Open IoT Challenge. In this context, several third parties projects adopted Kura IoT Framework.

http://iot.eclipse.org/open-iot-challenge/

Embedded World, February, 2015.

Innotrans, Berlin, September, 2014.

3.5.4 Other dissemination activities

Kura Open Sourcing:

Final version of Kura proposal released on 21/10/2013.

Kura is accepted as an Eclipse Project on 16/12/2013.

Kura 0.7.1 released on Sep 05th, 2014.

Kura 1.0.0 released on Sep 25th, 2014.

Kura 1.1.0 released on Dec 19th, 2014.

Kura 1.1.1 released on Feb 05th, 2015.

Kura 1.1.2 released on Apr 10th, 2015.

Kura Community Projects:

"Using Eclipse Kura, MQTT and CoAP to build a smart greenhouse", http://iot.eclipse.org/java/tutorial/

"Smart Helmet – Using Eclipse Kura",

http://byrebg.blogspot.in/2015/03/smart-helmet-using-eclipse-kura.html

"Creating a maker friendly DIY IoT home automation solution",

http://open-iot-challenge.bittailor.ch/2015/03/22/project-wrap-up/

"Cloud vehicle monitoring system CARRACHO",

http://diyapps.blogspot.it/2015/03/eclipse-open-iot-challenge-final-post.html

Several project are available at the following link:

https://tobiddev.wordpress.com/

"Configure IoT Gateway Applications with Kura",

http://www.bitreactive.com/kura-config/

3.6 INTECS

3.6.1 Internal Events

Intecs presented the CONTREX project and preliminary results to the Intecs Industrial Divisions during an internal workshop held in Pisa on 12 November 2014.

3.6.2 Other dissemination activities

- Dissemination has initiated by Intecs with members of the CONCERTO ARTEMIS project, coordinated by Intecs. CONCERTO aims at delivering a reference multi-domain architectural framework for complex, highly concurrent, and multi-core systems, where non-functional properties (including real-time, safety and dependability) will be established for individual components, derived for the overall system at design time, and preserved by construction and monitoring at run-time.
- In particular CONCERTO plans to adopt solutions from the CONTREX technical reports that describe the extensions proposed to MARTE for capturing MCS features and concerns.

3.7 iXtronics GmbH

3.7.1 Publications

Publications are planned for the second half of the project.

3.7.2 Presentations at Conferences / Workshops

A workshop within the master degree program in computer science of the Carl von Ossietzky University Oldenburg with the project group. This workshop is the basis for the project group Avionic Architecture. In the project group Avionic Architecture 12 students developed an avionics for a multi-rotor system, which is based on a Xilinx ZYNQ Multiprocessor System-on-Chip (MPSoC). The postulated result of the course was to get a stable flying system, which uses the processing power of the MPSoC not only for the

flight algorithms but also for another performance needing on-board task. The main focus of the workshop was on Model-driven development.

3.7.3 Exhibitions and Demonstrations

Demonstrations of intermediate implementations of the upcoming CAMeL-View-CONTREX-toolbox were performed for customers within internal events.

3.7.4 Internal Events

Several face-to-face meetings with different customers from the automotive and mechanical engineering industries. IX gave an outlook of the upcoming CAMeL-View-CONTREX-toolbox and discussed the new features with the customers.

3.8 EDALab

3.8.1 Publications

Filippo Cucchetto, Alessandro Lonardi, Graziano Pravadelli, A common architecture for co-simulation of SystemC models in QEMU and OVP virtual platforms in Proc. of IFIP/IEEE International Conference on Very Large Scale Integration , Proc. of IFIP/IEEE International Conference on Very Large Scale Integration, Playa del Carmen, Mexico, 6-8 October, 2014, pp. 67-72

Sara Vinco, Alessandro Sassone, Franco Fummi, Enrico Macii, Massimo Poncino, An Open-Source Framework for Formal Specification and Simulation of Electrical Energy Systems, Proc. IEEE International Symposium on Low Power Electronics and Design (ISLPED), pp. 287-290, 2014

Michele Lora, Francesco Martinelli, Franco Fummi, Hardware Synthesis from Software-Oriented UML Descriptions, Proc. IEEE International Workshop on Microprocessor Test and Verification (MTV), Austin, TX, USA , 15–16 December, 2014

Alessandro Danese, Tara Ghasempouri, Graziano Pravadelli Automatic extraction of assertions from execution traces of behavioural models, Proc. of DATE 2015

Emad Ebeid, Franco Fummi, and Davide Quaglia, Model-Driven Design of Network Aspects of Distributed Embedded Systems, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. PP, n. 99, 2015, pp. 1-12, DOI 10.1109/TCAD.2015.2394395.

3.8.2 Presentations at Conferences / Workshops

Filippo Cucchetto, Alessandro Lonardi, Graziano Pravadelli, A common architecture for co-simulation of SystemC models in QEMU and OVP virtual platforms in Proc. of IFIP/IEEE International Conference on Very Large Scale Integration , Proc. of IFIP/IEEE International Conference on Very Large Scale Integration, Playa del Carmen, Mexico, 6-8 October, 2014, pp. 67-72

Sara Vinco, Alessandro Sassone, Franco Fummi, Enrico Macii, Massimo Poncino, An Open-Source Framework for Formal Specification and Simulation of Electrical Energy Systems, Proc. IEEE International Symposium on Low Power Electronics and Design (ISLPED), pp. 287-290, 2014

Michele Lora, Francesco Martinelli, Franco Fummi, Hardware Synthesis from Software-Oriented UML Descriptions, Proc. IEEE International Workshop on Microprocessor Test and Verification (MTV), Austin, TX, USA , 15–16 December, 2014

Alessandro Danese, Tara Ghasempouri, Graziano Pravadelli Automatic extraction of assertions from execution traces of behavioural models, Proc. of DATE 2015

3.8.3 Exhibitions and Demonstrations

Alessandro Danese, Oden: Assertion Mining For Behavioral Descriptions, DATE University Booth, 2015

Graziano Pravadelli, OSTC: Combining Hifsuite And Scnsl For Smart Device Integration And Simulation, DATE University Booth, 2015

3.8.4 Other dissemination activities

Massimo Poncino, Davide Quaglia, Alain Pegatoquet, The power of Power in future wireless smart systems for the Internet of Things, DATE Tutorial, 2015

3.9 DOCEA POWER

3.9.1 Presentations at Conferences / Workshops

Gene Matter, Ilija Materic, Nicolas Peltier, Sylvian Kaiser, Power and Thermal Modeling and Analysis at the System Level, System to Silicon Performance Modeling and Analysis Workshop, DAC, 2014

Gene Matter, Sylvian Kaiser, ESL Power Simulation, Top Semiconductor Design Flow Challenges Panel, EDPS, 2014

3.9.2 Exhibitions and Demonstrations

Philippe Garrault*, Hela Boussetta*, Nicolas Peltier*, Tanguy Sassolas†, Julien Mottin†, Pascal Vivet†, (*DOCEA Power, †CEA-LIST/CEA-LETI), Early Validation of MPSoCs Thermal Mitigation Using a Thermal Aware Virtual Platform - The STHORM Circuit & Board Demonstration, DAC, 2014

Lionel Blanc, Ilija Materic, Jean-Christophe Oudin, Power Management Trade-off Analysis Using an Architectural-Level Power Model, DAC, 2014

3.9.3 Other dissemination activities

Presentation to the consortium of the CATRENE OpenES project, for the purpose of project cross-fertilization

3.10 POLITECNICO DI MILANO

3.10.1 Publications

Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. “DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling”. In Proceedings of DATE 2014 - International Conference on Design, Automation and Test in Europe. Dresden, Germany. March 2014.

Edoardo Paone, Davide Gadioli, Gianluca Palermo, Vittorio Zaccaria e Cristina Silvano. “Evaluating Orthogonality between Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications”. In Proceedings of ASAP - International Conference on Application-specific Systems, Architectures and Processors. Zurich, Switzerland. June 2014.

Mariagiovanna Sami, Gianluca Palermo. “Virtual Semi-Concurrent Self-Checking for Heterogeneous MPSoC Architectures: A DSE Approach” In Proceedings of ASAP - International Conference on Application-specific Systems, Architectures and Processors. Zurich, Switzerland. June 2014.

Carlo Brandolese, Luigi Rucco, William Fornaciari. Optimal wakeups clustering for highly-efficient operation of WSNs periodic applications. IEEE international conference on information communication and embedded systems (ICICES). Chennai, Tamilnadu, India, February 2014.

Carlo Brandolese, Luigi Rucco, William Fornaciari. An optimal model to partition the evolution of periodic tasks in wireless sensor networks. IEEE international symposium on a world of wireless mobile and multimedia networks. Sydney, Australia, June 2014.

Edoardo Paone, Francesco Robino, Gianluca Palermo, Vittorio Zaccaria, Ingo Sander and Cristina Silvano. “Customization of OpenCL Applications for Efficient Task Mapping under Heterogeneous Platform Constraints” Accepted in DATE 2015 – Design Automation and Test in Europe 2015.

Fernando Herrera, Ingo Sander, Kathrin Rosvall, Edoardo Paone, Gianluca Palermo “An Efficient Joint Analytical and Simulation-based Design Space Exploration Flow for Predictable Multi-Core Systems” RAPIDO15 - 7th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools. Amsterdam, The Netherlands, January 2015.

Amir Hossein, Ashouri; Giovanni, Mariani; Gianluca, Palermo and Cristina, Silvano; “A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processors”, ESTIMedia'2014 - IEEE Symposium on Embedded Systems for Real-Time Multimedia. New Delhi, India, October 2014.

Patrick Bellasi, Giuseppe Massari, and William Fornaciari. 2015. Effective Runtime Resource Management Using Linux Control Groups with the BarbequeRTRM Framework. ACM Trans. Embed. Comput. Syst. 14, 2, Article 39 (March 2015), 17 pages.

Simone Libutti, Giuseppe Massari, William Fornaciari “Addressing Task Co-scheduling on Multi-core Heterogeneous Systems: An Energy-Aware Perspective ” HIPEAC Workshop on Energy Efficiency with Heterogeneous Computing (EEHCO), Jan. 19 2015, Amsterdam

3.10.2 Presentations at Conferences / Workshops

The paper "DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling" has been presented by Gianluca Palermo at DATE 2014 Dresden, Germany. March 2014. The event is very large, however the audience of the session was around 40 people.

Gianluca Palermo presented a poster at HIPEAC 2014 (Jan 2014, Vienna, Austria) on "DRuiD: Designing Reconfigurable Architectures with Decision-making Support" describing the usage of Machine Learning techniques in HW/SW application mapping for FPGA based designs. Globally the event included more than 400 people. Among them with around 10-15 researchers and PhD students a detailed technical discussion have been done on the content of the poster.

On the same events Gianluca Palermo as co-organizer of the RAPIDO workshop, moderated an invited talk session on functional and extra-functional modelling of multicore platform where a presentation of CONTREX given by Philipp Hartmann from OFFIS has been included. The audience of the RAPIDO workshop during the invited session was around 40 people from both industry and academia.

Carlo Brandolese presented the paper "Optimal wakeups clustering for highly-efficient operation of WSNs periodic applications" at ICICES2014. The number of attendees of the event was around 200 peoples, 30 people were in the specific session where the paper has been presented.

Gianluca Palermo presented the paper "Evaluating Orthogonality between Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications" in ASAP14 within the IBM site in Zurich. The number of attendees was around 80 people for the session. In the same event Gianluca Palermo presented also a poster titled "Virtual Semi-Concurrent Self-Checking for Heterogeneous MPSoC Architectures: A DSE Approach" that attracted 10-15 researchers to discuss deeply on the topic.

The paper "Customization of OpenCL Applications for Efficient Task Mapping under Heterogeneous Platform Constraints" has been presented by Gianluca Palermo at DATE 2015 in Grenoble France March 2015. This work have been developed as a collaboration between KTH and PoliMi, and raised lot of interest among the audience. The event is very large, however the audience of the session was around 60 people.

Gianluca Palermo presented the paper "A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processors" in ESTIMEDIA within the Embedded System Week in New Delhi. The number of attendees of the session was around 40 peoples coming from both industries and academia.

Gianluca Palermo as co-organizer of the RAPIDO workshop co-located with HIPEAC 2015 (Jan 2015, Amsterdam), moderated an invited talk session on modelling extra-functional properties on multicore architectures to increase the attention on this CONTREX key aspect. The audience of the RAPIDO workshop during the invited session was around 30 people from both industry and academia

3.10.3 Exhibitions and Demonstrations

No presentations or demo has been done at exhibitions so far.

3.10.4 Internal Events

CONTREX related tools developed at POLIMI have been outlined during some master degree level courses at POLIMI: Embedded System Design, Advanced Operating Systems and Advanced Computer Architectures.

Internal Seminars to the POLIMI research group not involved in the project including also MSc, Graduate and PhD students:

- Davide Gadioli. "ARGO: A C++ framework for monitoring application level extra-functional properties and supporting application auto-tuning". April 2014.
- Edoardo Paone: "Improving DSE with Constraint Programming techniques for efficient DoE definition (Report of the period at KTH)". January 2014.
- Gianluca Palermo: "Automatic Design Space Exploration using MOST". September 2014.
- Amir Ashouri. "Compiler Auto-tuning: a DSE approach". July 2014.
- Edoardo Paone. "Using DSE for run-time adaptation". June 2014.
- Giuseppe Massari "BBQ-RTRM: Effective Runtime Resource Management Using Linux Control Groups" September 2014.
- Gianluca Palermo. "Joint Analytical-Simulation based DSE for Mixed critical systems". January 2015.
- Gianluca Palermo "Customization of OpenCL Applications for Efficient Task Mapping under Heterogeneous Platform Constraints". April 2015

3.11 POLITECNICO DI TORINO

3.11.1 Publications

- S. Vinco, A. Sassone, D. Lasorsa, E. Macii, M.Poncino.
  "A Framework for Efficient Evaluation and Comparison of EES Models,"
  PATMOS'14: Power and Timing Modeling, Optimization and Simulation, Palma de Mallorca, September 2014, pp.1—8.
- M. Petricca, A. Sassone, D. Shin, A. Bocca, A. Macii, E. Macii, M. Poncino,
  ``Automated Generation of Battery Aging Models from Datasheets,''
  ICCD'14: *IEEE International Conference on Computer Design*, October 2014, pp. 483-488.

3.11.2 Presentations at Conferences / Workshops

We have presented papers at the following conferences (including the two above papers)

- Alessandro Sassone (Grenoble, France, July 2014)
  "An Efficient Simulation Methodology for Electrical Energy Systems"
  PRIME-14: IEEE Conference on Ph.D. Research in Microelectronics and Electronics
  (reported in D6.3.2)
- M. Poncino (San Diego, USA, August 2014)
  "An Open-Source Framework for Formal Specification and Simulation of Electrical Energy Systems"
  ISLPED'14*: International Symposium on Low power Electronics and Design*(reported in D6.3.2)
- S. Vinco (Palma, Spain, September 2014)
  "A Framework for Efficient Evaluation and Comparison of EES Models,"
  PATMOS'14: Power and Timing Modeling, Optimization and Simulation, Palma de Mallorca, September 2014, pp.1—8.
- D. Shin (Seoul, Korea, October 2014)
  "Automated Generation of Battery Aging Models from Datasheets"
  ICCD'14: *IEEE International Conference on Computer Design*, October 2014, pp. 483-488.

3.11.3 Exhibitions and Demonstrations

No presentation has been done at exhibitions so far.

3.11.4 Internal Events

The Open-Source Framework described in the first publication is currently used in course in the Master program in Computer Engineering taught by Prof. Poncino at POLITO (course for the academic year 2014/2015 finished in January 2015). This course that targets embedded systems, the students use a model-based approach to design complete systems including power source, energy storage devices and various digital and non-digital electronic components, and where the target property to be simulated is power.

3.12 UNIVERSIDAD DE CANTABRIA

3.12.1 Publications

- Fernando Herrera (UC), Kathrin Rosvall, Ingo Sander (KTH), Edoardo Paone and Gianluca Palermo (PoliMi). "An Efficient Joint Analytical and Simulation-based Design Space Exploration Flow for Predictable Multi-Core Systems". In RAPIDO'15 7th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools 21 Jan 2015, Amsterdam, The Netherlands.

3.12.2 Presentations at Conferences / Workshops

- J. Medina . "A synthesis of modeling needs and the solutions proposed in CONTREX". Mixed Criticality Project Cluster Workhsop. July 2nd, 2014. Brussels, Belgium.

- Medina J.L., González Harbour M., Gutiérrez JJ.., Palencia J.C., Cuevas C., López P., and Drake J.M.. Experiencing the multi-path schedulability analysis capabilities in MAST 1.5. In Proc. of Forum on Design and Specification Languages 2014, pp 175-176. Munich, Germany, October 14th-16th, 2014.

- F. Herrera. RAPIDO Workshop paper presentation in HiPEAC 2015. Jan 2015, Amsterdam, The Netherlands.

- F. Herrera. Poster presentation of the first version of the JAS-DSE methodology in HiPEAC 2015: https://www.youtube.com/watch?v=lHKzfH5hOmU

3.12.3 Other dissemination activities

In the CONTREX Technical meeting hold in Oldenburg in December 2014, the CONTREX UML/MARTE modelling methodology (in its current status) was presented. The preliminary version of the JAS-DSE methodology was also presented.

- Proff. E. Villar co-chaired the Special Session on Mixed-Criticality System Design, Implementation and Analysis (MCSDIA) in EUROMICRO DSD/SEAA 2014, hold in Verona, Italy, August 27-29, 2014.

3.13 KUNGLIGA TEKNISKA HOEGSKOLAN

3.13.1 Publications

F. Herrera, K. Rosvall, I. Sander, E. Paone, and G. Palermo. An efficient joint analytical and simulation-based design space exploration flow for predictable multi-core systems. In *Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO)*, Amsterdam, The Netherlands, Jan. 2015.

F. Herrera and I. Sander. *Languages, Design Methods, and Tools for Electronic System Design*, chapter Combining Analytical and Simulation-Based Design Space Exploration for Efficient Time-Critical and Mixed-Criticality Systems, pages 167-188. 2015.

3.13.2 Internal Events

The following seminars and lectures are strongly related to CONTREX WP2. In particular they take up the problems of shared resources, the use of models of computation, the ForSyDe modelling libraries and the analytical design space exploration technique used in CONTREX.

Seminar at KTH/EES/AC: Ingo Sander. *Formal Software Design of Predictable Embedded Multiprocessor Applications*. Feb 6, 2015. (12 attendees, academia)

Seminar at KTH/ICT/SCS: Ingo Sander. *Correct-by-Construction Design of Embedded Real-Time Multiprocessor Applications*. Feb 26, 2015. (25 attendees, mainly academia)

Lectures as part of IL2212 Embedded Software (master course, KTH, 45 students):

- System Design with ForSyDe (90 minutes)
- Correct-by-Construction Design of Embedded Real-Time Multiprocessor Applications (90 minutes)
- A constraint-based design space exploration framework for real-time applications on MPSoCs (45 minutes)

3.13.3 Other dissemination activities

The following presentations are strongly related to CONTREX WP2. In particular they take up the problems of shared resources, the use of models of computation, the ForSyDe modelling libraries and the analytical design space exploration technique used in CONTREX.

- Invited seminar at Ångpanneföreningen (ÅF, Swedish consulting company): Ingo Sander. *Towards a Formal Software Design Methodology for Predictable Embedded Multiprocessor Applications*. Nov 11, 2014. (25 attendees, industry)
- Workshop between KTH and DTU, Feb 17-18, 2015: Ingo Sander. Correct-by-Construction Design of Embedded Real-Time Multiprocessor Applications. (8 attendees, academia)

3.14 ST-POLITO

3.14.1 Other dissemination activities

During this period, ST-Polito prepared ad-hoc material to disseminate CONTREX activities and results trough various means, including participation to tutorials and seminars. ST-Polito will promote the project results by the means of presentations held both internally and to some of its strategic customers. Specific trainings, to ST colleagues, customers and students, will complement these activities.

4 Relations to Other Projects

A strengthened relation has been developed with the OpenES project:

- CONTREX objectives, approach and expected results has been presented to the whole OpenES consortium (by the common partner Docea Power)
- The workshop on System to Silicon Performance Modeling and Analysis at DAC 2015 has been developed in tight cooperation with OpenES
- A Forum Workshop is planned together with OpenES at the major European industry event DVCon Europe (to be organized in November 2015 in conjunction with the DVCon Europe Conference)

Within the MCC cluster, several activities were planned and jointly organized:

- First MCC Workshop
- Common Special Session at the FDL 2015 Conference
- Booth with posters at the ARTEMIS Co-Summit

Some activities relative to the development of model for power source, converters and energy storage devices as well as their fitting into a SystemC/IP-XACT based simulation framework partially inherit from project FP7-ICT-288827 “SMAC” (Smart Systems Co-design),in which the focus is however on functional properties. The extension to non-functional properties and firstly to power/energy is the focus of POLITO’s contribution to CONTREX.

5 Summary

In this reporting period, CONTREX has undertaken several constructive dissemination activities that were thought to create a community wide awareness and cooperation between the most valuable partners, consortia and industries.

Some of the most valuable dissemination actions undertaken in the first reporting period will be continued and strengthened in the next period:

- MCC Cluster workshops and special sessions at FDL will continue to be a crucial part of the wide-dissemination activities
- System-to-Silicon Performance Modeling and Analysis Workshop will mobilize the international world-wide community and offer a platform for exchange ideas and promote solutions (including initiation of standardization activities)

In addition to all dissemination activities described in the present document, CONTREX will organize a Forum Workshop at the largest industrial event in the system design/verification area – the DVCon Europe Conference. This specific action will create a major dissemination opportunity for CONTREX to gain industrial visibility and help to increase project impact on the entire community (methodology advances, standardization efforts, share of results and exploitation.