FP7-ICT-2013- 10 (611146)  CONTREX

Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties

Project Duration 2013-10-01 – 2016-09-30  Type IP

<table>
<thead>
<tr>
<th>WP no.</th>
<th>Deliverable no.</th>
<th>Lead participant</th>
</tr>
</thead>
<tbody>
<tr>
<td>WP6</td>
<td>D6.4.2</td>
<td>ECSI</td>
</tr>
</tbody>
</table>

CONTREX Forum Report (Intermediate)

Prepared by Adam Morawiec (ECSI)
& Ralph Goerjen (OFFIS)

Issued by ECSI

Document Number/Rev. CONTREX/EC8I/D/D6.4.2/1.0

Classification CONTREX Public

Submission Date 2015-05-11
Due Date 2015-03-31

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2013)

© Copyright 2015 OFFIS e.V., STMicroelectronics srl, GMV Aerospace and Defence SA, Cobra Telematics SA, Eurotech SPA, Intecs SPA, iXtronics GmbH, EDALab srl, Docea Power, Politecnico di Milano, Politecnico di Torino, Universidad de Cantabria, Kungliga Tekniska Hoegskolan, European Electronic Chips & Systems design Initiative, ST-Polito Societa’ consortile a r.l..

This document may be copied freely for use in the public domain. Sections of it may be copied provided that acknowledgement is given of this original work. No responsibility is assumed by CONTREX or its members for any application or design, nor for any infringements of patents or rights of others which may result from the use of this document.
## History of Changes

<table>
<thead>
<tr>
<th>ED.</th>
<th>REV.</th>
<th>DATE</th>
<th>PAGES</th>
<th>REASON FOR CHANGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>AM</td>
<td>0.1</td>
<td>2015-04-08</td>
<td>10</td>
<td>Initial version</td>
</tr>
<tr>
<td>AM</td>
<td>1.0</td>
<td>2015-05-08</td>
<td>24</td>
<td>Final version</td>
</tr>
</tbody>
</table>
Contents

1 Introduction .................................................................................................................. 4
2 MCC Workshop 2014 in Brussels .................................................................................. 5
   2.1 Workshop Agenda .................................................................................................. 6
3 MCC Forum Website ..................................................................................................... 7
4 Special Session at EUROMICRO DSD/SEAA 2014 .................................................... 8
   4.1 Call for Papers and Scope ...................................................................................... 8
   4.2 Program Committee ............................................................................................... 9
   4.3 Program .................................................................................................................. 10
5 Workshop “MCS: Integration of mixed-criticality subsystems on multi-core and
   manycore processors” at HiPEAC Conference .............................................................. 11
   5.1 Organizers .............................................................................................................. 11
   5.2 Workshop Program ............................................................................................... 12
   5.3 Community Session .............................................................................................. 13
6 ARTEMIS/ITEA Co-Summit 2015 ............................................................................ 16
   6.1 MCC Exhibition Booth .......................................................................................... 17
   6.2 MCC Speakers Corner .......................................................................................... 17
7 DAC Workshop ............................................................................................................ 19
   7.1 Introduction ........................................................................................................... 19
   7.2 Workshop Program ............................................................................................... 21
8 CONTREX Forum Workshop at DVCon Europe .......................................................... 24
1 Introduction

In this document we present the progressive activities to establish the CONTREX Forum.

In its initial idea, the Forum was planned to largely disseminate project results, but also initiate discussion on partial results, get feedback from larger number of industry members, than those involved in the CONTREX consortium.

CONTREX step-wise creates the momentum around the crucial problems addressed by the project, with particular emphasis on mixed-criticality and extra-functional properties modelling and analysis. Focused workshops and events were organized by the CONTREX consortium to mobilise the community around these topics. In the next step the Forum event will be organized. After a thorough analysis of the potential opportunities to organize such an event in the industry context, a specific event was clearly selected in the area of electronic systems design and verification: the DVCon Europe event. In order to strengthen the impact, the CONTREX Forum event will be organized in tight cooperation with the OpenES project.
2 MCC Workshop 2014 in Brussels

The European mixed-criticality cluster consisting of the three EU FP7 projects CONTREX, DREAMS and PROXIMA organised an internal workshop that took place on July 2nd in Brussels. The workshop aimed the mutual technical understanding of planned work in the projects as well as to present first research results in the projects, to identify synergies in future standardisation activities and to foster the collaboration in between the cluster.

All three projects contributed to the workshop with 12 technical presentations and a total of about 50 attendees. CONTREX contributed with the following two presentations:

- Modelling of Distributed Embedded Mixed-Critical Systems
- Analysis of extra-functional properties power, temperature, and degradation in MCS
## 2.1 Workshop Agenda

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Project</th>
<th>Speaker</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>09:00</td>
<td>Welcome and Overview</td>
<td></td>
<td>Roman Obermaisser, Francisco Cazorla, Kim Grüttnner</td>
<td>Welcome</td>
</tr>
<tr>
<td>09:10</td>
<td></td>
<td></td>
<td>Roman Obermaisser, Francisco Cazorla, Sven Rosinger</td>
<td>Project overviews</td>
</tr>
<tr>
<td>09:40</td>
<td>Certification</td>
<td>DREAMS, PROXIMA</td>
<td>Leire Rubio, IKERLAN</td>
<td>Towards Modular Certification of Mixed-Criticality Systems</td>
</tr>
<tr>
<td>10:00</td>
<td></td>
<td>PROXIMA</td>
<td>Jon Perez/Mikel Azkarate, IKERLAN</td>
<td>e.g. Certification arguments based on probabilistic chip-level platforms</td>
</tr>
<tr>
<td>10:20</td>
<td>Scheduling and Timing</td>
<td>DREAMS</td>
<td>Gerhard Fohler, TUKL</td>
<td>Resource management and scheduling for MCS</td>
</tr>
<tr>
<td>10:40</td>
<td>Analysis</td>
<td>PROXIMA</td>
<td>Mark Pearce (RAPITA), Enrico Mezzetti (University of Padua)</td>
<td>e.g. Probabilistic timing analysis for multi-cores</td>
</tr>
<tr>
<td>11:00</td>
<td>Morning Coffee Break</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:30</td>
<td></td>
<td>DREAMS</td>
<td>Hamidreza Ahmadian, USIEGEN</td>
<td>TSP and Heterogeneous Models of Computation at Chip-Level</td>
</tr>
<tr>
<td>11:50</td>
<td></td>
<td>DREAMS</td>
<td>Marcello Coppola, ST</td>
<td>Memory Interleaving</td>
</tr>
<tr>
<td>12:10</td>
<td></td>
<td>PROXIMA</td>
<td>Jaume Abella</td>
<td>e.g. Chip-Level Platform for probabilistic WCET guarantees</td>
</tr>
<tr>
<td>12:30</td>
<td>Lunch Break</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13:30</td>
<td>Model-Driven Development</td>
<td>CONTREX</td>
<td>Julio Medina, Universidad de Cantabria</td>
<td>Modelling of Distributed Embedded Mixed-Critical Systems</td>
</tr>
<tr>
<td>13:50</td>
<td></td>
<td>DREAMS</td>
<td>Simon Barner, FORTISS</td>
<td>Dev. process for MCS and modelling of Networked Multi-Core Chips</td>
</tr>
<tr>
<td>14:10</td>
<td></td>
<td>DREAMS</td>
<td>Oystein Haugen, SINTEF</td>
<td>Variability modelling</td>
</tr>
<tr>
<td>14:30</td>
<td>Extra functional</td>
<td>CONTREX</td>
<td>Sven Rosinger, OFFIS</td>
<td>Analysis of extra-functional properties power, temperature, and degradation in MCS</td>
</tr>
<tr>
<td>14:50</td>
<td>properties</td>
<td>DREAMS</td>
<td>Thomas Koller, USIEGEN</td>
<td>Security in MCS</td>
</tr>
<tr>
<td>15:10</td>
<td>Afternoon Coffee Break</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:40</td>
<td>Community Platform</td>
<td>DREAMS</td>
<td>Arjan Geven, TTT</td>
<td>MCS Community Platform</td>
</tr>
<tr>
<td>16:30</td>
<td>Panel discussion on</td>
<td>DREAMS, PROXIMA, EU</td>
<td>Moderator: Alfons Crespo, UPV</td>
<td>Open exploitation, joint exploitation, IP issues, ...</td>
</tr>
<tr>
<td>17:30</td>
<td>Impact and Exploitation</td>
<td></td>
<td>Roman Obermaisser</td>
<td>Workshop closure</td>
</tr>
</tbody>
</table>
3 MCC Forum Website

The CONTREX project participated in the set-up of the Mixed-Criticality Cluster Forum website. It is available at the following address:

http://www.mixedcriticalityforum.org
4 Special Session at EUROMICRO DSD/SEAA 2014

The 17\textsuperscript{th} Euromicro Conference on Digital System Design has taken place in Verona, Italy, in August 27-29, 2014. It addresses all aspects of (embedded, pervasive and high-performance) digital and mixed hardware/software system engineering, down to microarchitectures, digital circuits and VLSI techniques.

As part of the conference, the “Special Session on Mixed-Criticality System Design, Implementation and Analysis (MCSDIA)” has been organized Kim Grüttner and Eugenio Villar with the help of other CONTREX and MCC partners.

4.1 Call for Papers and Scope

Modern embedded appliances already integrate a multitude of functionalities with potentially different criticality levels into a single system and this trend is expected to grow in the near future. The integration of multiple functions with different criticality and certification assurance levels on a shared computing platform constitutes a mixed-criticality system (MCS). Mixed-criticality systems range from lowest assurance requirements up to the highest criticality levels (e.g., DAL A in RTCA DO-178B or SIL4 in EN ISO/IEC 61508 and 26262). In many domains such as automotive, avionics and industrial control, the economic success depends on the ability to design, implement, qualify and certify advanced real-time embedded systems within bounded time, effort and costs. Without appropriate preconditions, the integration of mixed-criticality subsystems can lead to a significant and potentially unacceptable increase of engineering and certification costs. There are several ongoing research initiatives studying mixed-criticality integration in single and multicore processors, as well as on distributed systems. Key challenges are the combination of software virtualization and hardware segregation and the extension of partitioning mechanisms jointly addressing significant extra-functional requirements (e.g., time, energy and power budgets, adaptivity, reliability, safety, security, volume, weight, etc.) along with a proven development and certification methodology. To support the design and implementation of mixed-criticality systems, new design techniques and tools for the analysis of extra-functional properties are required.

Special Session Scope

This special session aims at gathering contributions regarding the design, implementation and analysis of mixed-criticality systems within a dedicated forum. Papers on any of the following and related topics will be considered for the special session:

- Task and system models for mixed-criticality systems on single and multicore platforms,
- mechanisms for temporal and spatial partitioning, physical resource virtualization for temporal and spatial segregation, resource partitioning to achieve composability in multiple dimensions (time, power, temperature, …), solutions for shared communication resource partitioning, resources partitioning techniques at chip and cluster level, dynamic resource management for services of mixed-criticality, multi-physical component- and model-based design techniques, (composable) analysis of extra-functional properties (like timing, power, temperature, safety and security), reliability and energy integrity of services with mixed-criticality, dependable operation of battery-driven/mobile mixed-criticality systems, requirements engineering and traceability for mixed-criticality systems, modular safety cases, (incremental) verification of extra-functional properties, composable certification techniques,
design-space exploration for multi-physical mixed-criticality systems, and industrial case-studies.

4.2 Program Committee

4.2.1 Session Co-Chairs:
- Kim Grüttnner, OFFIS – Institute for Information Technology, Germany
- Eugenio Villar, University of Cantabria, Spain

4.2.2 Special Session Program Subcommittee:
- Sanjoy Baruah, The University of North Carolina, USA
- Gedare Bloom, The George Washington University, USA
- Francisco J. Cazorla, Supercomputing Center and IIIA-CSIC, Spain
- Arvind Easwaran, Nanyang Technological University, Singapore
- William Fornaciari, Politecnico di Milano, Italy
- Franco Fummi, University of Verona, Italy
- Kees Goossens, Eindhoven University of Technology, The Netherlands
- Philipp A. Hartmann, OFFIS – Institute for Information Technology, Germany
- Knut Hufeld, Infineon Technologies AG, Germany
- Silvia Mazzini, INTECS, Italy
- Julio Medina, University of Cantabria, Spain
- Moritz Neukirchner, TU Braunschweig, Germany
- Roman Obermaisser, University of Siegen, Germany
- Ingo Sander, KTH, Sweden
- Ingo Stierand, Carl von Ossietzky University Oldenburg, Germany
- Jean-Loup Terraillon, ESA, The Netherlands
- Salvador Trujillo, IK4-IKERLAN Research Centre, Spain
- Andreas von Schwerin, Siemens AG, Germany
- Roberto Zafalon, STMicroelectronics, Italy
4.3 Program

Mixed Criticality System Design, Implementation and Analysis 1 (MCSDIA1)

Thursday, 28 August 2014, 10:00 – 11:00


Mixed Criticality System Design, Implementation and Analysis 2 (MCSDIA2)

Thursday, 28 August 2014, 15:30 – 16:30

- “A safety certification strategy for IEC-61508 compliant industrial mixed-criticality systems based on multicore partitioning” Jon Perez, David Gonzalez, Carlos Fernando Nicolas, Ton Trapman and Jose Miguel Garate

5 Workshop “MCS: Integration of mixed-criticality subsystems on multi-core and manycore processors” at HiPEAC Conference

The 10th HiPEAC conference has taken place in Amsterdam, The Netherlands from Monday, January 19 to Wednesday, January 21, 2015. As part of this conference, the workshop “MCS: Integration of mixed-criticality subsystems on multi-core and manycore processors” has been held on Monday. The workshop has been attended by 103 people from 69 different institutions.

The MCS community aims to solve the challenges to safely integrate applications and systems of higher and lower criticality together on multicore and distributed architectures. In order to safely achieve this, challenges reside at the hardware and software architecture level as well as in the support by means of methodology, modelling, simulation, verification, documentation and training.

5.1 Organizers
- Francisco Cazorla (Barcelona Supercomputing Center),
- Jon Perez (IK4-IKERLAN),
- Kim Grüttner (OFFIS),
- Roman Obermaisser (University of Siegen),
- Sascha Uhrig (University of Dortmund)
5.2 Workshop Program

10:00-10:05 “Welcome and Introduction” (Dr. Jon Perez – IK4-IKERLAN)

10:05-11:00 Mixed-Criticality Platform (Dr. Francisco Cazorla – BSC)

- "Segregation of Subsystems with Different Criticalities on Networked Multi-Core Chips in the DREAMS Architecture” (Roman Obermaisser – University of Siegen, FP7 Project DREAMS)
- “Embedded Mixed Criticality Multicore – An industry perspective of multicore and certification” (Bernd Koppenhoefer – Airbus Defence and Space, ARTEMIS Project EMC²)

11:00-11:30 Coffee Break

11:30-11:45 Mixed-Criticality Platform (Dr. Francisco Cazorla – BSC)

- “Mixed criticality for complex networked systems” (Arjan Geven – TTTech, FP7 Project DREAMS)

11:45-13:00 Community building (Dr. Roman Obermaisser – University of Siegen)

- “The vision of the commission” – Presented by Werner Steinhögl (Programme Officer; Complex Systems and Advanced Computing CONNECT – A3; European Commission)
- Mixed-Criticality community building (Arjan Geven – TTTech)
- Community building interactive part (Arjan Geven – TTTech)

15:00-16:00 Certification (Dr. Roman Obermaisser – University of Siegen)

- “Towards modular certification of mixed-criticality product lines based on multicore and virtualization technology (IEC-61508) – Wind power and railway case studies” (Jon Perez – IK4-Ikerlan, FP7 Projects MultiPARTES / DREAMS / PROXIMA)
- “XtratuM Hypervisor: certification elements” (Alfons Crespo – UPV, FP7 Projects MultiPARTES / DREAMS)

16:00-16:30 Tools and MBD design methods (Kim Grüttner – OFFIS)

- “Towards power, temperature and aging analysis and estimation for SoCs at system-level” (Kim Grüttner – OFFIS, FP7 Project CONTREX)

16:30-17:00 Coffee Break

17:00-18:00 Tools and MBD design methods (Kim Grüttner – OFFIS)

- “Probabilistic timing analysis for multicore based mixed-criticality systems” (Francisco Cazorla – BSC, FP7 Project PROXIMA)
5.3 Community Session

Along with the workshop, a community session was held focusing on the advancement of the Mixed-Criticality Forum and Community. With a total of roughly 50 engaged participants from academia and industry across Europe, the workshop can be considered successful with fruitful discussions. Discussions were centred on three central themes: expectations, content, and potential barriers.

The session was organized from the context of the Mixed-Criticality Forum at http://mixedcriticalityforum.org, an initiative within the FP7 project DREAMS to support the ‘Mixed-Criticality Cluster’ of ongoing FP7 projects, i.e. DREAMS, CONTREX and PROXIMA and the growing mixed-criticality community in academia and industry.

The results of the three discussion groups are summarized in the following.

**Group 1: Expectations to the Mixed-Criticality Community**

(10 participants)

In the first group, the discussions focused on the expectations of the participants towards a mixed-criticality community. The general comment is that the MCF can become a reference repository for researchers in MCS in different aspects.
- **Requirements/Metrics**: There was a general feeling that academics can be looking into problems of small interest to industry. This can be corrected/prevented by asking different industries (across different domains) to articulate a document with their main requirements in terms of timing, reliability, and any other metric of interest. This will also help academics to understand what can be done (and what can be assumed) when attacking a problem and what cannot.

- **Overview of standards**: In this respect, it is understood that many requirements come from standards, which are hard to read. However, from the dozens of standards in a domain, the experts in the domain know which are those apply for the problem under interest and the particular paragraphs in those standards that are of interest. It would be great if this information is put in the MCF website.

- **Best practices for MCS**: A document with Best Practices in each domain would also be of help. This document cover the main elements to take into account when deploying a software/hardware function that is to be deployed in the targeted application domain.

- **Experiences with MCS**: This part covers experiences of people (likely industrialists) on multicore mixed-criticality systems. The feeling is that a lot can be learnt from the experience of other people with MCS. Further, overlaps can be found among different domains.

- **Who is doing what in the community**: This section covers a good description of what each member of the MCF is doing: in the different application domains and in the different layers of the computing system. This would help industry understanding who is doing what in the Mixed-Criticality community. This helps looking for partners for new projects and building connection among partners.

**Group 2: Technical contents**

(24 participants)

In the second group, the discussions focused on the technical contents and potential contributions of parties involved in research on Mixed-Criticality Systems. Regrettably, time was too short to go into detailed discussions about specific technical contributions. The discussions therefore centred on the organization of the contents within the MCF and how to further enable the contribution of technical content.

- **Application domains**: the definition of mixed criticality as well as the challenges and expectation from the solutions are very diverse in the different domains. All provided content should be linked with an industrial domain. For this purpose, it might be useful to collect the domains covered by the MCC projects.

- **Use cases**: to provide (high-level) use-cases of industrial mixed-criticality problems from the domains avionics and railway. These use-cases can be used to identify common challenges and join forces to work on the solutions. Anyhow, there might be some confidentiality issues that need to be discussed internally first.

- **Common requirements**: A common list on requirements (maybe per domain) for mixed-criticality system could be collected and harmonized across the MCF contributors (each project should have done this anyhow)

- **Terminology**: A common definition and a refined definition of “Mixed-Criticality” in the different domains could give some guidance to new players entering the scene.

- **Industrial best-practices**: Guidelines, procedures and best practices from industrial partners could be collected and published through the MCF.

- **Security**: Guidelines what you need to consider would be well received. Specific input from the EURO-MILS (http://www.euromils.eu/) project has been offered. They have
developed a matrix to compare different safety and security critical systems. This could be a valuable contribution to the MCF.

- **Collection of standards and certification bodies** per domain could be very interesting. The MCF could also become a common place to discuss potential shortcomings and roadblocks of existing standards.

Furthermore, potential additions to the MCF were discussed to further broaden the scope and usefulness of the Mixed-Criticality Forum. In particular, the following were mentioned:

- **Publication and deliverable database**: A database of publications from each project of the MCC. Each Bibtex entry would also carry: a link to the project(s) of the MCC, a link to the industrial domain or the common domain, and a pdf, if possible. This publication database could be Bibtex-based. The database could further be extended with a Public deliverable database of all deliverables from each MCC project to facilitate the interaction between the projects.

- **Social functions**: the group discussed about ways to further facilitate the social interaction between organizations and projects, e.g. the integration of a full discussion forum and mailing list for discussions, and the integration with social media by means of Facebook Fan Page and Twitter Channel.

Group 3: Barriers to adoption
(15 participants)
Within the MCS community, several barriers to the adoption of MCS solutions identified that can be addressed at least in part by community activities. In the group, the following topics were discussed:

- **Common Terminology**: A missing common terminology is perceived as a barrier. For example, there are different definitions of mixed-criticality systems in different communities (e.g., scheduling community vs. certification). In addition, consolidation of terminology from different domains (automotive, avionics, ...) and different technological communities (e.g., real-time, high-performance, ...) is necessary.

- **Certification standards**: High certification cost is a barrier towards the certification of multi-core systems. Certification standards need updates to enable the certification of these systems.

- **Ecosystem**: Project results need to be leveraged after research projects finish.

- **Distance between academic and industry**: There is a gap between industrial challenges and academic research. The level of ambition in academic research is often far from industrial state-of-practice and actual industrial challenges.

- **Fail-safe and fail-operational systems**: Both fail-safe and fail-operational systems need to be addressed. Mixed-criticality research at present focuses on fail operational systems.
6 ARTEMIS/ITEA Co-Summit 2015

The seventh edition of the annual Co-summit “Smart Industry: impact of software innovation” took place at the Berlin Congress Center on 10/11 of March 2015. The Co-summit was jointly organised by ITEA, the EUREKA Cluster on Software-intensive Systems & Services and by ARTEMIS Industry Association, the association for actors in Embedded & Cyber-Physical Systems within Europe.

Over two days a diversity of projects, presentations and discussions demonstrated the central and crucial role played by ITEA and ARTEMIS projects in the creation of new, smart manufacturing and processing. In her keynote address, Jutta Schneider, Director of eDrive and Software Technologies at Daimler AG, underlined the importance of “software innovation as a key driver”, a view that was resoundingly echoed by other prominent speakers from the German government, the European Commission and industry. During the panel discussion on the Co-summit theme, TNO’s Egbert-Jan Sol suggested that “it is not simply so-ftware innovation but also business innovation and social innovation” that are keys to the evolutionary process that is revolutionising industry. Importantly, Thomas Lagerberg of ABB put the question: “We have all these big data and connectivity but it is important to ask what’s in it for me, how can I make money out of it? We have to demonstrate the benefits to people.”

Examples of precisely such benefits were being displayed all around the exhibition floor: ARTEMIS and ITEA projects that not only captured the imagination but actually showed to more than 700 visitors and participants the tangible impact of their work. Like the R5-COP autonomous WALL•E-looking robot wandering around the exhibition floor, an example of a smart solution for dirty and dangerous jobs, or the BaaS project leaders in their hardhats and hazard warning vests that attracted interest in the use of novel value-added services and applications for smart commercial buildings – both winners of the Exhibition Award.

Speakers corners offered insight into smart industry trends, such as the future of automated driving with a focus on secure connectivity and the role of Cyber-Physical Systems as a key technology in the connectivity. Or the dilemma of financing healthcare in which Philips believes that by cleverly linking Cyber-Physical Systems the costs of realising requirements for the healthcare system chain can be reduced. Speakers from as far as Canada and South Africa underlined the global dimension of the Co-summit and the European programmes.

The CONTREX project participated in this event together with the other Mixed Criticality Cluster projects DREAMS and PROXIMA. On one hand, there was a joint MCC exhibition booth to promote the Mixed Criticality Cluster and the project topics. On the other hand, the cluster organized a speakers corner with presentations and discussions on mixed-criticality systems.
6.1 MCC Exhibition Booth

6.2 MCC Speakers Corner

The speakers corner with the title “Towards Platforms for Mixed-Criticality Systems” on mixed-criticality systems was held on 10 March 2015 with the following agenda:

14:00 - 16:00 Towards Platforms for Mixed-Criticality Systems

14:00 - 14:05 Mixed-Criticality Systems and Research Challenges

14:05 - 14:15 Vision of the European Commission

Multi-Core Platforms for Mixed-Criticality Systems

14:15 - 14:30 DREAMS - EC FP7

14:30 - 14:45 PROXIMA - EC FP7

14:45 - 15:00 EMC2 - ARTEMIS

15:00 - 15:15 P-SOCRATES - EC FP7

Development Methodologies for Mixed-Criticality Systems

15:15 - 15:30 CRYSTAL - ARTEMIS
15:30 - 15:45  CONTREX - EC FP7
15:45 - 16:00  MBAT - ARTEMIS
7 DAC Workshop

7.1 Introduction

This is the second workshop organized jointly by CONTREX and OpenES projects to create the momentum in the community around the aspects of modelling of extra-functional properties. The objective for both projects is to exchange information on advances and results, but also to present them to the industry in general sense. This is why the workshop is organized in the context of the major international conference DAC (Design Automation Conference) to gain exposure to major industry players.

This year also the presentations in the workshop will be given by several partners outside of the project consortia including Intel, Xilinx, ARM, Cadence, IMEC, IROC, Toshiba and several renowned research partners.
System-to-Silicon Performance Modeling and Analysis

*Power, Temperature and Reliability*

DAC 2015 Workshop
June 7, 2015 - San Francisco, CA, USA

**Preliminary Program**

**Rationale**
The integration of heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional properties: timing, energy consumption, thermal behavior, reliability, cost and others as well as performance aspects related to caching, non-determinism, probabilistic effects.
The workshop addresses cross-domain aspects related to the design and verification framework covering methodology, interoperable tools, flows, interfaces and standards that enable formalization, specification, annotation and refinement of functional and extra-functional properties of a system. Special emphasis will be given to formalization and expression of power, temperature, reliability, degradation and aging.
Several research and industry efforts address (parts of) the problem. However, there is a need for community-wide cooperation to establish a holistic vision on extra-functional property treatment, and to agree on research and development directions and further on validation of applicable solutions and standardization.
This event will support collaboration between main actors from system and microelectronics industry, EDA and research.
The workshop is inviting submissions of short abstracts industrial and scientific work in progress and practical solution and experiences.

**Workshop Organizers:**
- Laurent Maillet-Conoz, STMicroelectronics, France
- Kim Grüttner, OFFIS, Germany
- Gjalt de Jong, ArchWorks, Belgium
- Adam Morawiec, ECSI, France

**Session Organizers:**
- Andreas Herkersdorf, TU München, Germany
- Jürgen Becker, KIT Karlsruhe, Germany
- Domenik Helms, OFFIS, Germany
- Christoph Sohrmann, Fraunhofer Institute for Integrated Circuits IIS, Germany
- Roland Jancke, Fraunhofer Institute for Integrated Circuits IIS, Germany

Organized by projects:
## 7.2 Workshop Program

<table>
<thead>
<tr>
<th>Time</th>
<th>Session/Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:00</td>
<td>Intro &amp; Welcome &amp; Agenda</td>
</tr>
<tr>
<td>9:05</td>
<td>Keynote</td>
</tr>
<tr>
<td>9:50</td>
<td><strong>Session 1</strong> System-Level Design for Reliability</td>
</tr>
<tr>
<td></td>
<td><strong>Organizers:</strong> Andreas Herkersdorf (TU München, Germany), Jürgen Becker (KIT Karlsruhe, Germany)</td>
</tr>
<tr>
<td></td>
<td><strong>Abstract:</strong> Reliability is a system-level concern, both from the hardware/software architecture as well as design method perspectives. Advanced nanometer CMOS technologies are known to be increasingly vulnerable for radiation induced sporadic soft-errors, device aging and various forms of manufacturing and environmental variations. Another source of reliability exposures for today’s and future Systems-on-Chip (SoC) solutions is their inherent complexity, expressed either in Billions of transistors, number of IP cores integrated, and the variety of high functionality implemented on a single SoC. Today, it is already practically infeasible to validate such SoCs down to clock cycle accuracy under various representative workload scenarios. Both, feature size and complexity induced challenges cannot be addressed at individual, specific abstraction layers with acceptable quality and cost. Senior university and industry researchers from the US and Europe will share their perspectives on crucial design aspects of today’s and future embedded and cyber physical systems. Topics span from dependable NoC communication virtualization on MPSoC, to self-aware Cyber Physical Systems-on-Chip, to high-throughput database query acceleration on reconfigurable FPGAs with High-Level Synthesis, to reliability management of 3D stacked wireless baseband SoCs.</td>
</tr>
<tr>
<td>9:50</td>
<td>1.1 A Cross Layer Approach for Efficient Reliability Management in 3D Stacked Wireless Baseband SoCs Norbert Wehn (Microelectronic System Design Research Group, University of Kaiserslautern, Germany)</td>
</tr>
<tr>
<td>10:15</td>
<td>1.2 Using Roofline Models to Analyze the Performance of Realistic Key Value Store Implementations on FPGAs with High Level Synthesis Kees Vissers and Michaela Blott (Xilinx, USA and Ireland)</td>
</tr>
<tr>
<td>11:05</td>
<td>Coffee Break</td>
</tr>
<tr>
<td>11:20</td>
<td>1.4 Intel Euro Labs Presentation (TBC) Enno Lübbers, Intel Euro Labs, München, Germany</td>
</tr>
<tr>
<td>11:45</td>
<td>1.5 Enabling Dependable MPSoC Task Migration with On-Chip Interconnect Virtualization Andreas Herkersdorf (Integrated Systems Lab, Technische Universität München, Germany)</td>
</tr>
<tr>
<td>12:10</td>
<td>1.6 Dynamic Migration and Performance Optimization of Deterministic Applications Across Platform Components Using Intel® CoFluent™ Studio Jérôme Lemaître, Rocco Le Moigne (Intel Corporation SAS, France)</td>
</tr>
<tr>
<td>12:35</td>
<td>Lunch Break</td>
</tr>
<tr>
<td>13:15</td>
<td>Keynote</td>
</tr>
<tr>
<td>14:00</td>
<td><strong>Session 2</strong> Tools and Methods for Power and Temperature Modeling and Analysis</td>
</tr>
<tr>
<td></td>
<td><strong>Organizers:</strong> Kim Grüttnner (OFFIS, Germany), Domenik Helms (OFFIS, Germany), Laurent Maillet-Contoz (STMicroelectronics, France)</td>
</tr>
<tr>
<td></td>
<td><strong>Abstract:</strong> With the predicted device, core and multicore scaling, the dark silicon hypothesis predicts the end</td>
</tr>
</tbody>
</table>
of multicore scaling, regardless of chip organization and topology, due to power or energy density limitations. For this reason, future system engineers should be able to address power and thermal management as soon as possible in the design flow. Introduction of power and temperature management cannot be done at a single abstraction layer, but must be taken into consideration from the operating system, early system-level models, down to the integration of RTL IP components. For this reason, power and temperature properties need to be modelled across all abstraction layers, because they can strongly affect the products overall quality of service or even cause the system to fail meeting its real-time and safety requirements.

In this session will discuss breakthrough academic and industrial solutions to control power consumption and heat dissipation at design and run-time. Furthermore, this session will discuss proposed extensions of existing industrial standards and their implications on commercial tool support. The addressed topics are: operating system support for fine-grained system-level energy analysis through orchestration of energy measurements at hardware level; the extensions of IP-XACT and UPF industry standards to support a seamless ESL to RTL low power design methodology; the extension of IP-XACT with verification features including portable stimuli vectors to enable performance and power closure of complex SoCs; tools for architectural level power and thermal modeling; and a new thermal constrained run-time management called "Thermal Safe Power".

14:00 2.1 The FIGAROS Operating System Kernel for Fine-Grained System-Level Energy Analysis
Timo Hönig, Heiko Janker, Wolfgang Schröder-Preikschat (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany)

14:25 2.2 Extending IP-XACT and UPF to Support ESL to RTL Low Power Design Methodology
Emmanuel Vaumorin, Grégoire Avot (Magillem Design Services; France), Hend Affes, Michel Auguin, Alain Pégatoquet, François Verdier (Univ. Nice Sophia Antipolis)

14:50 Coffee Break

15:05 2.3 IP Configuration for the Right Balance Between Required Performance and Power
Nick Heaton (Cadence Design Systems, USA), Simon Rance (ARM, UK)

15:30 2.4 The Use of High Level IP Power Models Across System Analysis Environments and Teams
Sylvian Kaiser (Docea Power, France)

15:55 2.5 Thermal-Aware Power Budgeting for Dark Silicon Chips
Santiago Pagani, Muhammad Shafique (Karlsruhe Institute of Technology, Germany), Jian-Jia Cheny, Jörg Henkel (TU Dortmund, Germany)

16:20 Session 3 Ageing and Variation Prediction from Transistor to RT Level
Organizers: Christoph Sohrmann & Roland Jancke (Fraunhofer Institute for Integrated Circuits IIS, Germany)

Abstract:
Even in safety-critical areas such as Automotive, Aviation, Medical, and Industrial the demand for applications having highest performance, lowest energy consumption, and smallest dimensions together with extended service life grows rapidly. Combinations of these requirements can only be provided by extremely scaled technologies. Such safety-critical applications do not tolerate device failure. However, devices from advanced technology nodes are generally more susceptible to parametric deviations, either from process variations, parametric drift over lifetime or a combination thereof. The correct prediction of parametric deviations is similarly important as making them accessible on higher abstraction levels. The focus of this session are thus models and formats which abstract detailed knowledge about parameter variations and reliability from the device level to the circuit or RT level. The solutions presented will enable the designer to take these effects into account early in the design phase and ensure to meet specifications over the entire lifetime and for all application conditions.

16:20 3.1 Impact of Time-dependent Variability on the Yield and Performance of 6T SRAM Cells in an Advanced HK/MG Technology
Pieter Weckx, Ben Kaczer, Praveen Raghavan, Francky Catthoor, Guido Groeseneken (IMEC, Belgium)

16:45 3.2 Facilitating Cross-Layer Reliability Management through Universal Reliability
CONTREX/ECSI/D/D6.4.2/1.0

CONTREX Forum Report (Intermediate)

Information Exchange

Enrico Costenaro¹, Domenik Helms², Nematollah Bidokhti³, Adrian Evans¹, Maximilian Glorieux⁴ and Dan Alexandrescu¹ (¹IROC Technologies, France; ²OFFIS, Germany; ³OCZ Toshiba, USA)

17:10 3.3 Statistical Timing Methodology for Low-Power and Multi-Voltage Designs
Kerim Kalafala, Natesan Venkateswaran, Stephen Shuma, Vladimir Zolotov, Eric A Foreman (IBM Thomas J. Watson Research Center, USA)

17:35 3.4 Reliability-Driven Analog Circuit Design using gm/Id Method and Cross Layer Modelling of Aging
Steffen Paul, Nico Hellwege, Nils Heidmann, Dagmar Peters-Drolshagen (Institute of Electrodynamics and Microelectronics, ITEM, University Bremen, Germany)

18:00 Concluding Remarks & Closing
Adam Morawiec (ECSI)

CONTREX Contributions:

Keynote 1: An Accurate Simulation Framework for Thermal Explorations and Optimizations

Speaker: William Fornaciari (PolIMI, Italy)

Abstract:
While technology scaling allows integrating more cores in the same chip, the complexity of current designs requires accurate and fast techniques to explore different trade-offs. Moreover, the increased power densities in current architectures highlight thermal issues as a first class design metric to be addressed. At the same time, the need to access to accurate models for the exploited actuators is of paramount importance, since their overheads can shadow the benefit of the proposed methodologies. This talk proposes a complete simulation framework for the assessment of run-time policies for thermal-performance and power-performance trade-offs optimization with two main improvements over the state of the art. First, it accurately models Dynamic Voltage and Frequency Scaling (DVFS) modules for both cores and NoC routers as well as a complete Globally Asynchronous Locally Synchronous (GALS) design paradigm and power gating support for crossbar and buffers in the NoC. Second, it accounts for the chip thermal dynamics as well as power and performance overheads for the actuators. Some results related to the use of the framework for the identification of ultra-fast novel thermal management strategies and optimal design of NoC infrastructures will also be presented.

Presentation 2.4: The Use of High Level IP Power Models Across System Analysis Environments and Teams

Author: Sylvian Kaiser (Docea Power, France)

Abstract:
System behavior, and associated thermal behavior, directly impact the success of electronic products: cost, reliability, safety, quality of service, user experience, and compliance with industry standards. The design technology trend is yet making power and thermal more and more critical with higher power density, higher system integration and more power-hungry applications. In this context high abstraction level approaches can bring valuable system-wide observation and exploration of power behavior in advance of real physical systems, in order to make appropriate power-aware design trade-offs. In this paper we show how IP power models can be used in an architectural level modeling and simulation environment dedicated to SoC and platform power analysis. The environment allows spreadsheet-like static analysis and dynamic analysis, including early power-performance trade-off. The same IP power models can alternatively be used in high level behavioral and functional modeling platforms, for instance ESL platforms typically relying on SystemC-TLM, in order to augment the system simulation with a power estimation perspective. To help share and reuse the IP models across system modeling environments and across teams within an organization, a framework is set-up that centralizes and manages the models. The complete methodology generally improves a company's ability to address the system power dissipation concerns and launch products meeting or exceeding power targets.
8 CONTREX Forum Workshop at DVCon Europe

The CONTREX Workshop will be organized in conjunction with the DVCon Europe 2015 Conference and Exhibition to be organized on November 11-12, 2015 in Munich, Germany.

DVCon Europe Conference is considered by the CONTREX (and also OpenES) consortium as the most appropriate event to organize the Forum. It is mainly due to the several facts:

- DVCon Europe is the largest event in Europe related to the electronics systems design and verification methods:
  - Number of participants: 250
  - Number of exhibitors: 21 (with the largest EDA companies: Cadence, Mentor Graphics, Synopsys, OneSpin, AMIQ, Magillem, Docea, …)
  - Companies represented: 83
  - Papers presented: 27
  - Posters: 16
  - Tutorials presented: 14

- In 2015 it is expected that the conference will attract more than 350 attendees, and approx. 30 exhibitors

- The conference is owned and sponsored by the Accellera standardization organization. This creates an opportunity to initiate standardisation discussions and activities that can be used by the consortium to promote the project proposals to standardization.

More information on the conference can be found at www.dvcon-europe.org.